NEC

MOS INTEGRATED CIRCUIT

μPD78P368A

16/8 BIT SINGLE-CHIP MICROCOMPUTER

The μPD78P368A is produced by replacing the internal mask ROM of the μPD78366A with a one-time PROM or EPROM. One-time PROM products, in which data can be written once are effective for manufacture of small quantities of multiple products and early stage start-up of application. EPROM products, to which programs can be re-written after previously written programs have been erased, are suited for system evaluation.

The following user's manual describes the details of functions. Be sure to read it before design.

μPD78366A User's Manual, Hardware: U10205E

μPD78356 User's Manual, Instructions: IEU-1395

FEATURES

- Compatible with the μPD78366A
  - Can be replaced with the μPD78366A containing mask ROM on a full-production basis.
- Internal PROM: 48K bytes
  - Data can be written once (one-time PROM product without an erasure window)
  - Written data can be erased by exposure to ultraviolet light and re-written electrically (EPROM product with an erasure window)
- PROM programming characteristics: Compatible with the μPD27C1001A
- QTOP™ microcomputer

Remark The QTOP microcomputer is a single-chip microcomputer with a built-in one-time PROM that is totally supported by NEC. The support includes writing application programs, marking, screening, and verification.

ORDERING INFORMATION

Part number	Package	Internal ROM
μPD78P368AGF-3B9	80-pin plastic QFP (14 × 20 mm)	One-time PROM
μPD78P368AKL-S**Note**	80-pin ceramic WQFN	EPROM

Note Under development

In this manual, the description of the PROM is for both a one-time PROM and EPROM.

The information in this document is subject to change without notice.

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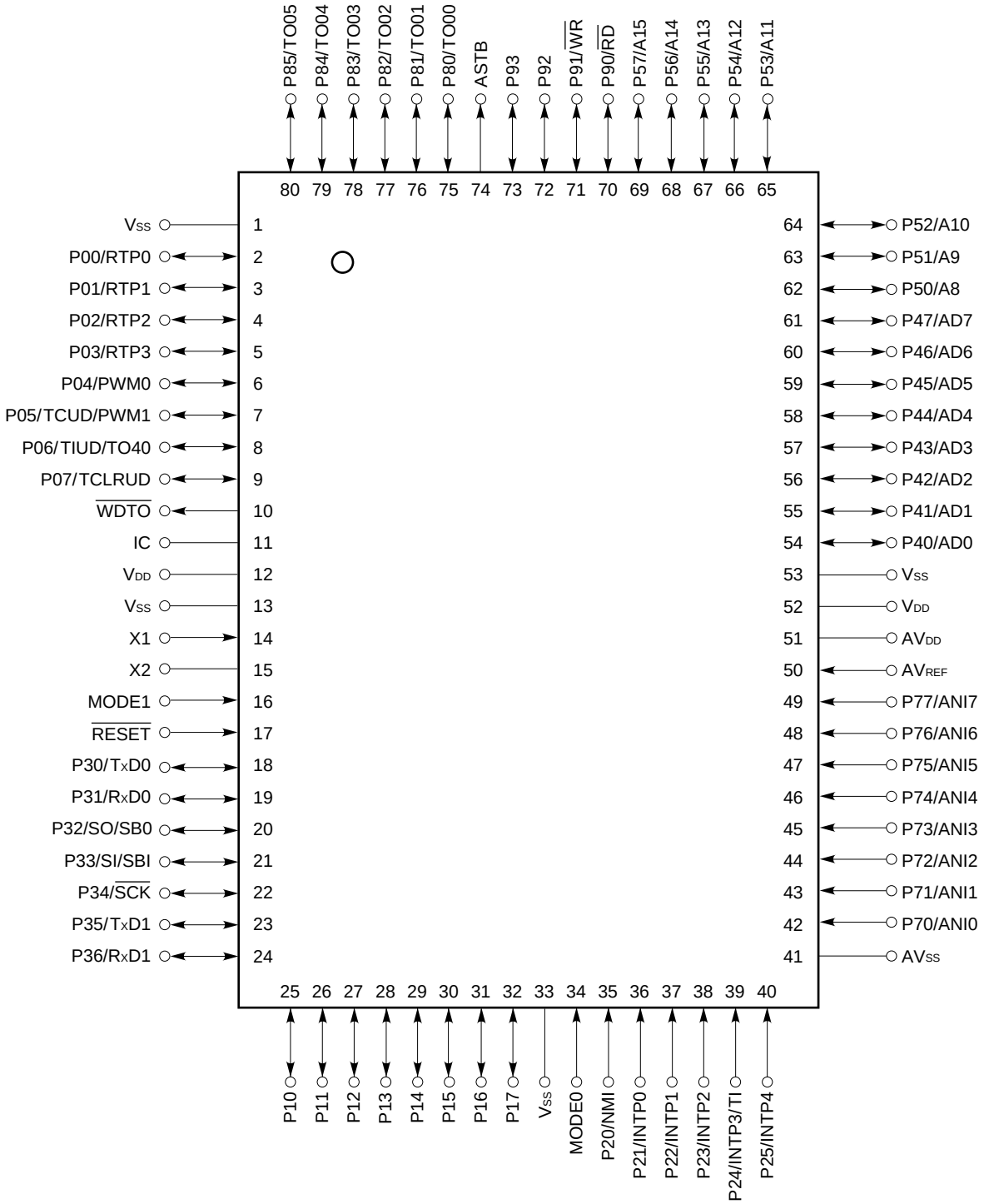
The mark ★ shows major revised points.

PIN CONFIGURATION (TOP VIEW)

(1) Normal operation mode (MODE0 = L, MODE1 = L)

- **80-pin plastic QFP (14 × 20 mm)**
  μPD78P368AGF-3B9
- **80-pin ceramic WQFN**
  μPD78P368AKL-S



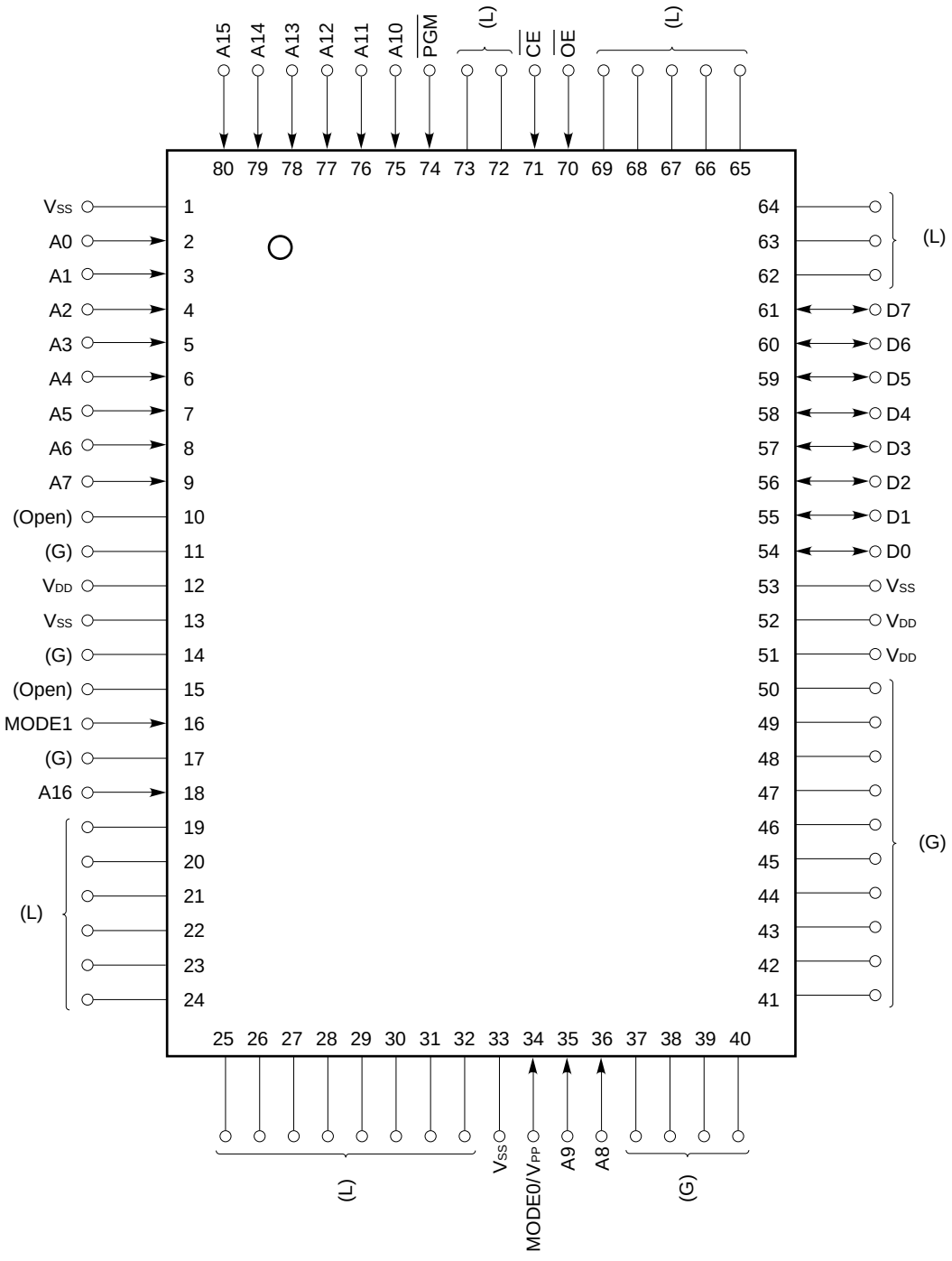
Caution Directly connect the IC pin to VSS.

Remark Pin compatible with the μPD78366AGF

P00-P07:	Port 0
P10-P17:	Port 1
P20-P25:	Port 2
P30-P36:	Port 3
P40-P47:	Port 4
P50-P57:	Port 5
P70-P77:	Port 7
P80-P85:	Port 8
P90-P93:	Port 9
RTP0-RTP3:	Real-time port
NMI:	Nonmaskable interrupt
INTP0-INTP4:	Interrupt from peripherals
TO00-TO05, TO40:	Timer output
TI:	Timer input
TIUD:	Timer input for up/down counter
TCUD:	Timer control for up/down counter
TCLRUD:	Timer clear for up/down counter
ANI0-ANI7:	Analog input
TxD0, TxD1:	Transmit data
RxD0, RxD1:	Receive data
SI:	Serial input
SO:	Serial output
SB0, SB1:	Serial bus
$\overline{SCK}$:	Serial clock
PWM0, PWM1:	Pulse width modulation output
$\overline{WDTO}$:	Watchdog timer output
MODE0, MODE1:	Mode
AD0-AD7:	Address/data bus
A8-A15:	Address bus
ASTB:	Address strobe
$\overline{RD}$:	Read strobe
$\overline{WR}$:	Write strobe
$\overline{RESET}$:	Reset
X1, X2:	Crystal
AV_{DD}:	Analog V_{DD}
AV_{SS}:	Analog V_{SS}
AV_{REF}:	Analog reference voltage
V_{DD}:	Power supply
V_{SS}:	Ground
IC:	Internally connected

(2) PROM programming mode (MODE0/V_{PP} = H, MODE1 = L)

- **80-pin plastic QFP (14 × 20 mm)**
  μPD78P368AGF-3B9
- **80-pin ceramic WQFN**
  μPD78P368AKL-S



Caution Symbols in parentheses denote how the pins not used in the PROM programming mode should be treated.

L: Connect these pins to the V_{SS} pins through separate resistors.

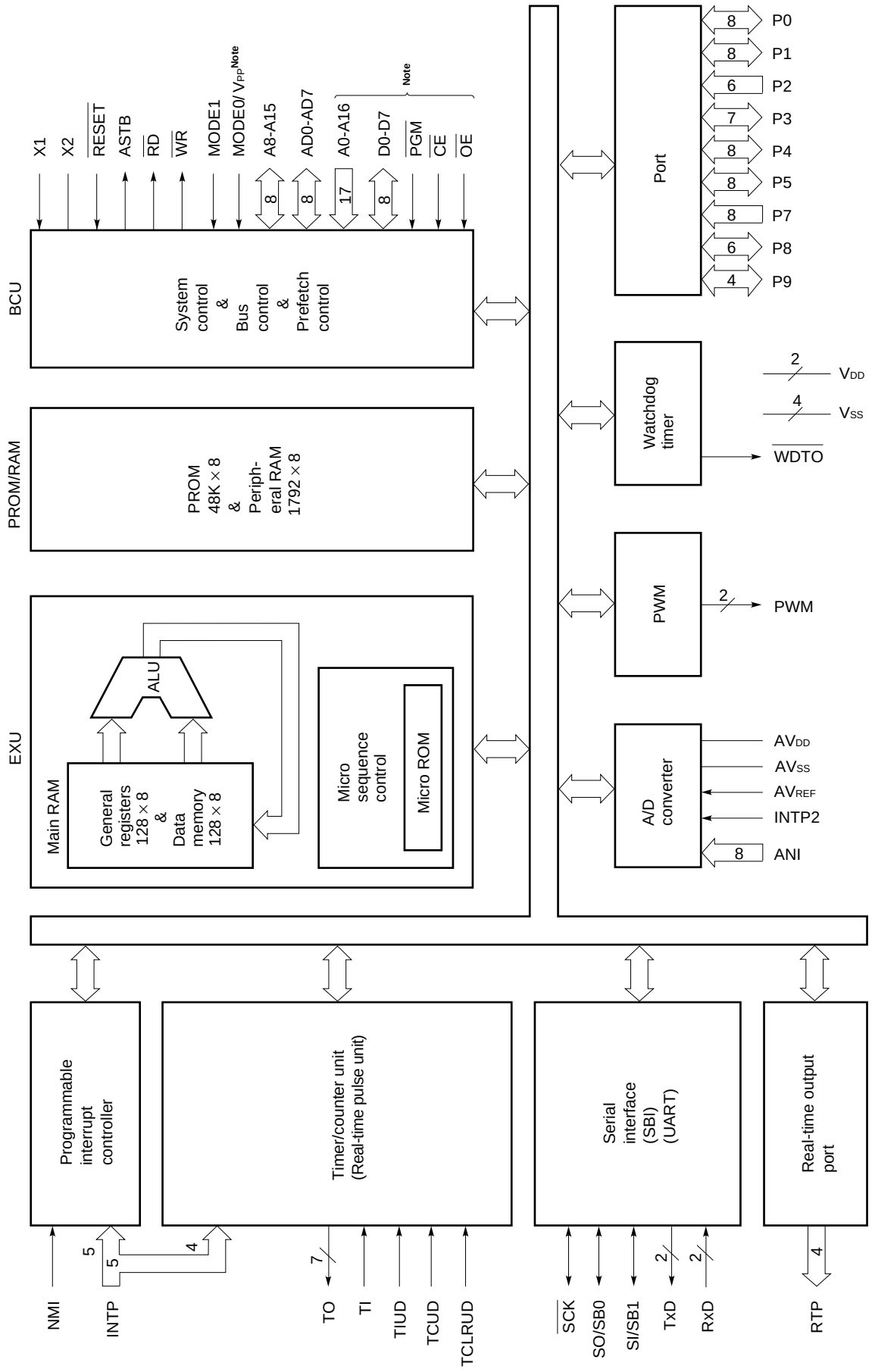
G: Connect these pins to the V_{SS} pins.

Open: Do not connect these pins to anything.

A0-A16: Address bus
D0-D7: Data bus
$\overline{CE}$: Chip enable
$\overline{OE}$: Output enable
$\overline{PGM}$: Programming mode

MODE0, MODE1: Programming mode set
V_{PP}: Programming power supply
V_{DD}: Power supply
V_{SS}: Ground

BLOCK DIAGRAM



Note Shading indicates the pins used in the PROM programming mode.

CONTENTS

1. PIN FUNCTIONS

1.1 NORMAL OPERATION MODE (MODE0 = L, MODE1 = L)

(1) Port pins

Pin name	I/O	Function	Dual-function pin
P00-P03	I/O	Port 0. 8-bit I/O port. Can be specified as input or output bit by bit.	RTP0-RTP3
P04			PWM0
P05			TCUD/PWM1
P06			TIUD/TO40
P07			TCLRUD
P10-P17	I/O	Port 1. 8-bit I/O port. Can be specified as input or output bit by bit.	–
P20	I	Port 2. Port used only for 6-bit input.	NMI
P21			INTP0
P22			INTP1
P23			INTP2
P24			INTP3/TI
P25			INTP4
P30	I/O	Port 3. 7-bit I/O port. Can be specified as input or output bit by bit.	TxD0
P31			RxD0
P32			SO/SB0
P33			SI/SB1
P34			$\overline{\text{SCK}}$
P35			TxD1
P36			RxD1
P40-P47	I/O	Port 4. 8-bit I/O port. Can be specified as input or output in units of 8 bits.	AD0-AD7
P50-P57	I/O	Port 5. 8-bit I/O port. Can be specified as input or output bit by bit.	A8-A15
P70-P77	I	Port 7. Port used only for 8-bit input.	ANI0-ANI7
P80-P85	I/O	Port 8. 6-bit I/O port. Can be specified as input or output bit by bit.	TO00 - TO05
P90	I/O	Port 9. 4-bit I/O port. Can be specified as input or output bit by bit.	$\overline{\text{RD}}$
P91			$\overline{\text{WR}}$
P92			–
P93			–

(2) Non-port pins (1/2)

Pin name	I/O	Function	Dual-function pin
RTP0-RTP3	O	Outputs a pulse in real time as triggered by a trigger signal sent from the real-time pulse unit.	P00-P03
NMI	I	Nonmaskable interrupt request input	P20
INTP0		External interrupt request input	P21
INTP1			P22
INTP2			P23
INTP3			P24/TI
INTP4			P25
TI	I	External count clock input to timer 1	P24/INTP3
TCUD		Input for the control signal to determine whether the up/down counter (timer 4) counts up or down.	P05/PWM1
TIUD		External count clock input to the up/down counter (timer 4)	P06/TO40
TCLRUD		Clear signal input to the up/down counter (timer 4)	P07
TO00-TO05	O	Pulse output from the real-time pulse unit	P80-P85
TO40			P06/TIUD
ANI0-ANI7	I	Analog input to the A/D converter	P70-P77
TxD0	O	Serial data output from the asynchronous serial interface	P30
TxD1			P35
RxD0	I	Serial data input to the asynchronous serial interface	P31
RxD1			P36
$\overline{SCK}$	I/O	Serial clock I/O for the clock synchronous serial interface	P34
SI	I	Serial data input to the clock synchronous serial interface in the 3-wire mode	P33/SB1
SO	O	Serial data output from the clock synchronous serial interface in the 3-wire mode	P32/SB0
SB0	I/O	Serial data I/O for the clock synchronous serial interface in the SBI mode	P32/SO
SB1			P33/SI
PWM0	O	PWM signal output	P04
PWM1			P05/TCUD
$\overline{WDTO}$	O	Output for the signal which indicates the watchdog timer overflowed. (A nonmaskable interrupt is generated.)	–
AD0-AD7	I/O	Multiplexed address/data bus used when external memory is expanded	P40-P47
A8-A15		Address bus used when external memory is expanded	P50-P57
ASTB	O	Output for the timing signal used in externally latching address information output from the AD0 to AD7 and A8 to A15 pins, in order to access the external memory	–
$\overline{RD}$		Read strobe signal output to the external memory	P90
$\overline{WR}$		Write strobe signal output to the external memory	P91

(2) Non-port pins (2/2)

Pin name	I/O	Function	Dual-function pin
MODE0	I	Input for the control signal which sets the operation mode. Normally, both MODE0 and MODE1 are directly connected to the V_{SS} pin.	–
MODE1			
$\overline{RESET}$	I	System reset input	–
X1	I	Crystal input pin for the system clock. A clock signal provided externally is input to the X1 pin. The reversed signal of the clock signal is input to the X2 pin.	–
X2	–		
AV_{REF}	I	A/D converter reference voltage input	–
AV_{DD}	–	Analog power supply for the A/D converter	–
AV_{SS}	–	Ground for the A/D converter	–
V_{DD}	–	Positive power supply	–
V_{SS}	–	Ground	–
IC	–	Internally connected. Directly connect the IC pin to V_{SS}.	–

1.2 PROM PROGRAMMING MODE (MODE0/V_{PP} = H, MODE1 = L)

Pin name	I/O	Function
MODE0/V_{PP}	I	PROM programming mode set/programming supply voltage
MODE1	I	PROM programming mode set
A0-A16	I	Address bus
D0-D7	I/O	Data bus
$\overline{PGM}$	I	Program input
$\overline{CE}$	I	Enable PROM
$\overline{OE}$	I	Read strobe to PROM
V_{DD}	–	Positive power supply
V_{SS}		GND

1.3 INPUT/OUTPUT CIRCUIT TYPE FOR EACH PIN AND HANDLING OF UNUSED PINS

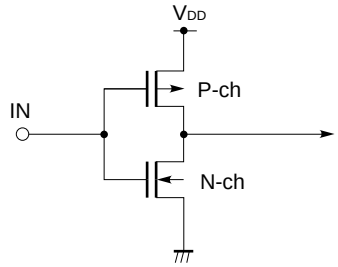
Table 1-1 lists the input and output circuit type for each pin and how to handle it when it is not used. Fig. 1-1 shows the circuits.

Table 1-1 Input/Output Circuit Type for Each Pin and Recommended Connection Methods for Unused Pins

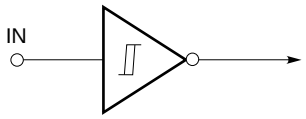
Pin	I/O circuit type	Recommended connection method
P00/RTP0-P03/RTP3	5-A	Input state: Each pin is connected to the V_{DD} or V_{SS} pin via a separate resistor. Output state: Open
P04/PWM0		
P05/TCUD/PWM1		
P06/TIUD/TO40		
P07/TCLRUD		
P10-P17		
P20/NMI	2	Connected to the V_{SS} pin.
P21/INTP0	2-A	
P22/INTP1		
P23/INTP2		
P24/INTP3/TI		
P25/INTP4		
P30/TxD0	5-A	Input state: Each pin is connected to the V_{DD} or V_{SS} pin via a separate resistor. Output state: Open
P31/RxD0		
P32/SO/SB0	8-A	
P33/SI/SB1		
P34/$\overline{SCK}$		
P35/TxD1	5-A	
P36/RxD1		
P40/AD0-P47/AD7		
P50/A8-P57/A15		
P70/ANI0-P77/ANI7	9	Connected to the V_{SS} pin.
P80/TO00-P85/TO05	5-A	Input state: Each pin is connected to the V_{DD} or V_{SS} pin via a separate resistor. Output state: Open
P90/$\overline{RD}$		
P91/$\overline{WR}$		
P92, P93		
ASTB	5	
$\overline{WDTO}$	19	Connected to the V_{SS} pin.
MODE0, MODE1	1	–
$\overline{RESET}$	2	
AV_{REF}, AV_{SS}	–	Connected to the V_{SS} pin.
AV_{DD}		Connected to the V_{DD} pin.

Fig. 1-1 Input/Output Circuits of Each Pin

Type 1

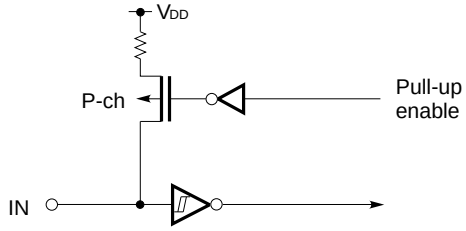


Type 2



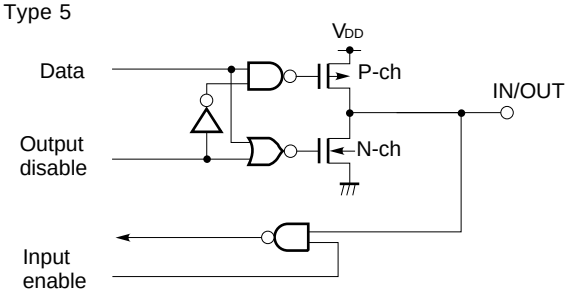
Schmitt trigger input with hysteresis characteristics

Type 2-A

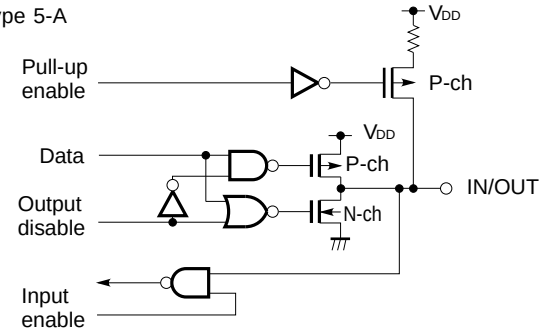


Schmitt trigger input with hysterisis characteristics

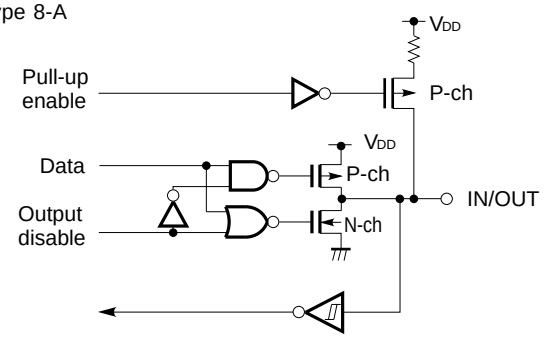
Type 5



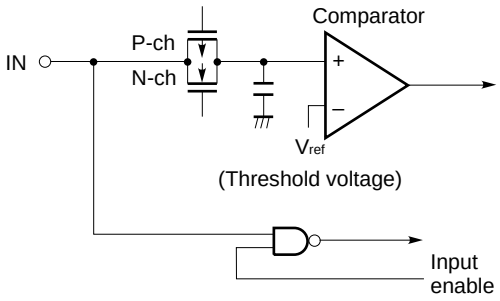
Type 5-A



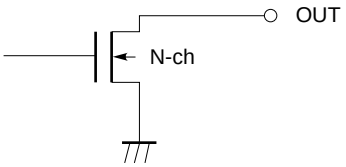
Type 8-A



Type 9



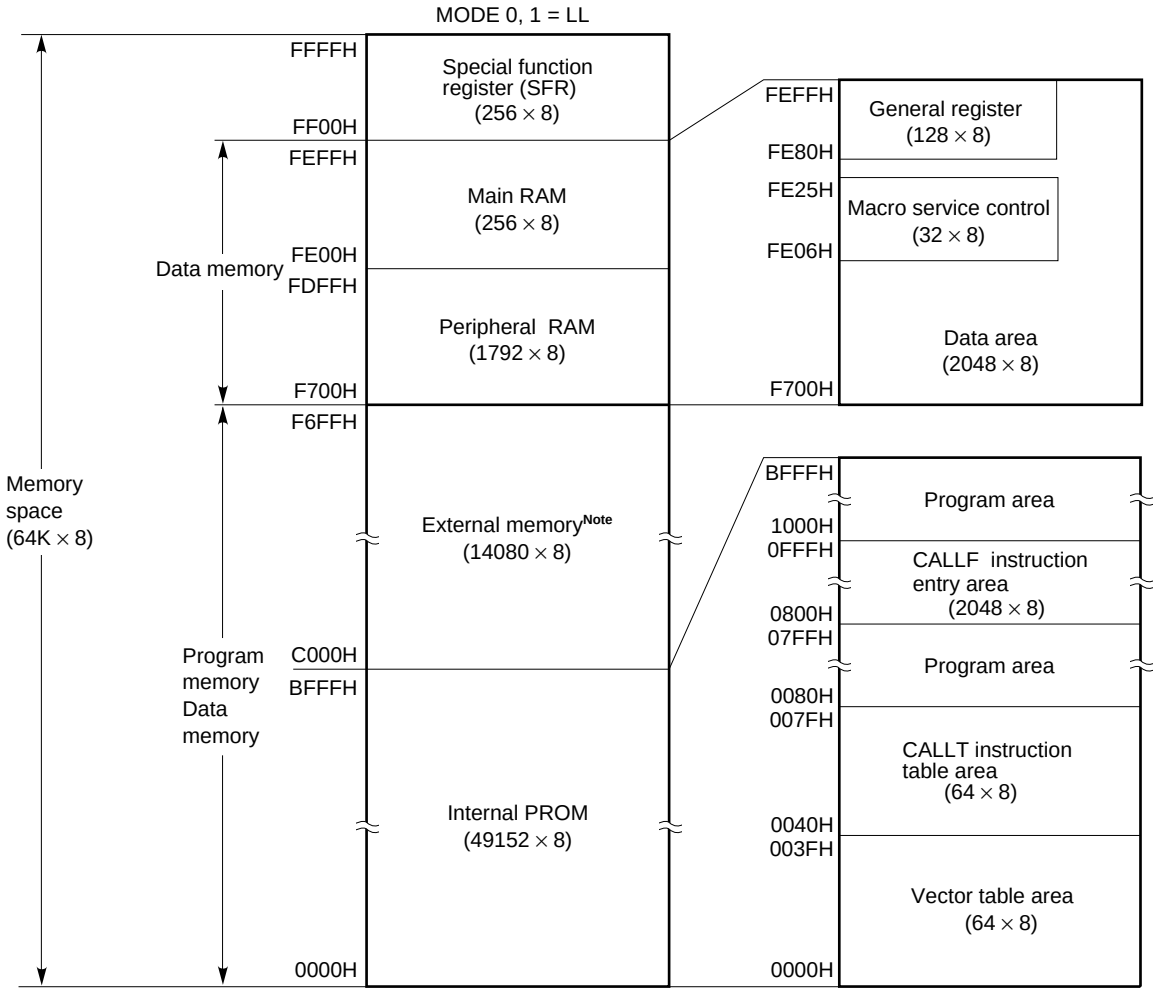
Type 19



2. MEMORY CONFIGURATION

The μPD78P368A can access memory of up to 64K bytes. Fig. 2-1 shows the memory map.

Fig. 2-1 Memory Map



Note Access in the external memory expansion mode.

Caution When word access (including the stack operation) to the main RAM space (FE00H to FEFFH) is executed, the addresses specified in the operand must be even numbers.

3. DIFFERENCES BETWEEN THE μPD78P368A AND μPD78366A

The μPD78P368A is produced by replacing the internal mask ROM of the μPD78366A with a 48K-byte PROM. Both have the same functions except some differences in ROM specifications, such as write and verify modes. Table 3-1 shows the differences.

In this manual, the functions specific to the μPD78P368A are explained. For details of the other functions, refer to the μPD78366A document.

Table 3-1 Differences between the μPD78P368A and μPD78366A

Item \ Part number	μPD78P368A		μPD78366A
ROM	48K bytes		32K bytes
Internal program memory (Electrical write)	One-time PROM (Data can be written once)	EPROM (Data can be written multiple times)	Mask ROM
PROM programming pin	Provided		Not provided
Setting of MODE0 and MODE1	• Normal operation mode MODE0, 1 = LL • PROM programming mode MODE0, 1 = HL		• Normal operation mode MODE0, 1 = LL • ROM-less mode MODE0, 1 = HH
Package	80-pin plastic QFP	80-pin ceramic WQFN	80-pin plastic QFP
Electrical characteristics	They differ in supply current and other factors.		
Others	Since each product has a different circuit scale and mask layout, the noise immunity and noise radiation of each product differ.		

Cautions 1. The PROM and mask ROM products differ in noise immunity and noise radiation. Use not ES products but CS products (mask ROM products) to evaluate them thoroughly when considering the change from the PROM products to the mask ROM products during processes from preproduction to volume production.

2. Connect the MODE0 and MODE1 pins directly to the V_{DD} or V_{SS} pin.

4. PROM PROGRAMMING

The μPD78P368A is provided with an electrically writable PROM of 48K × 8 bits. When programming this PROM, use the MODE0/V_{PP} and MODE1 pins to set the μPD78P368A to the PROM programming mode.

The μPD78P368A provides programming characteristics compatibility with the μPD27C1001A.

Table 4-1 Pin Functions in Programming Mode

Function	Normal operation mode	Programming mode
Address input	P00-P07, P21, P20, P80-P85, P30	A0-A16
Data input	P40-P47	D0-D7
Program pulse	ASTB	$\overline{PGM}$
Chip enable	P91	$\overline{CE}$
Output enable	P90	$\overline{OE}$
Program voltage	MODE0/V_{PP}	
Mode control	MODE1	

4.1 OPERATION MODE

To enter the program write/verify mode, set each pin as follows: MODE0/V_{PP} = H, MODE1 = L. In addition, any of the operation modes listed in Table 4-2 can be selected by setting the $\overline{CE}$, $\overline{OE}$, and $\overline{PGM}$ pins in this mode.

Set the μPD78P368A to the read mode in order to read the contents of PROM.

Handle unused pins as described in PIN CONFIGURATION (2).

Table 4-2 Operation Modes for PROM Programming

Mode	MODE1	$\overline{CE}$	$\overline{OE}$	$\overline{PGM}$	MODE0/V_{PP}	V_{DD}	D0-D7
Page data latch	L	H	L	H	+12.5 V	+6.5 V	Data input
Page program		H	H	L			High impedance
Byte program		L	H	L			Data input
Program verify		L	L	H			Data output
Program inhibit		×	L	L			High impedance
		×	H	H			
Read		L	L	H	+5 V	+5 V	Data output
Output disable		L	H	×			High impedance
Standby		H	×	×			High impedance

Remark ×: L or H

4.2 PROCEDURE FOR WRITING ON PROM (PAGE PROGRAM MODE)

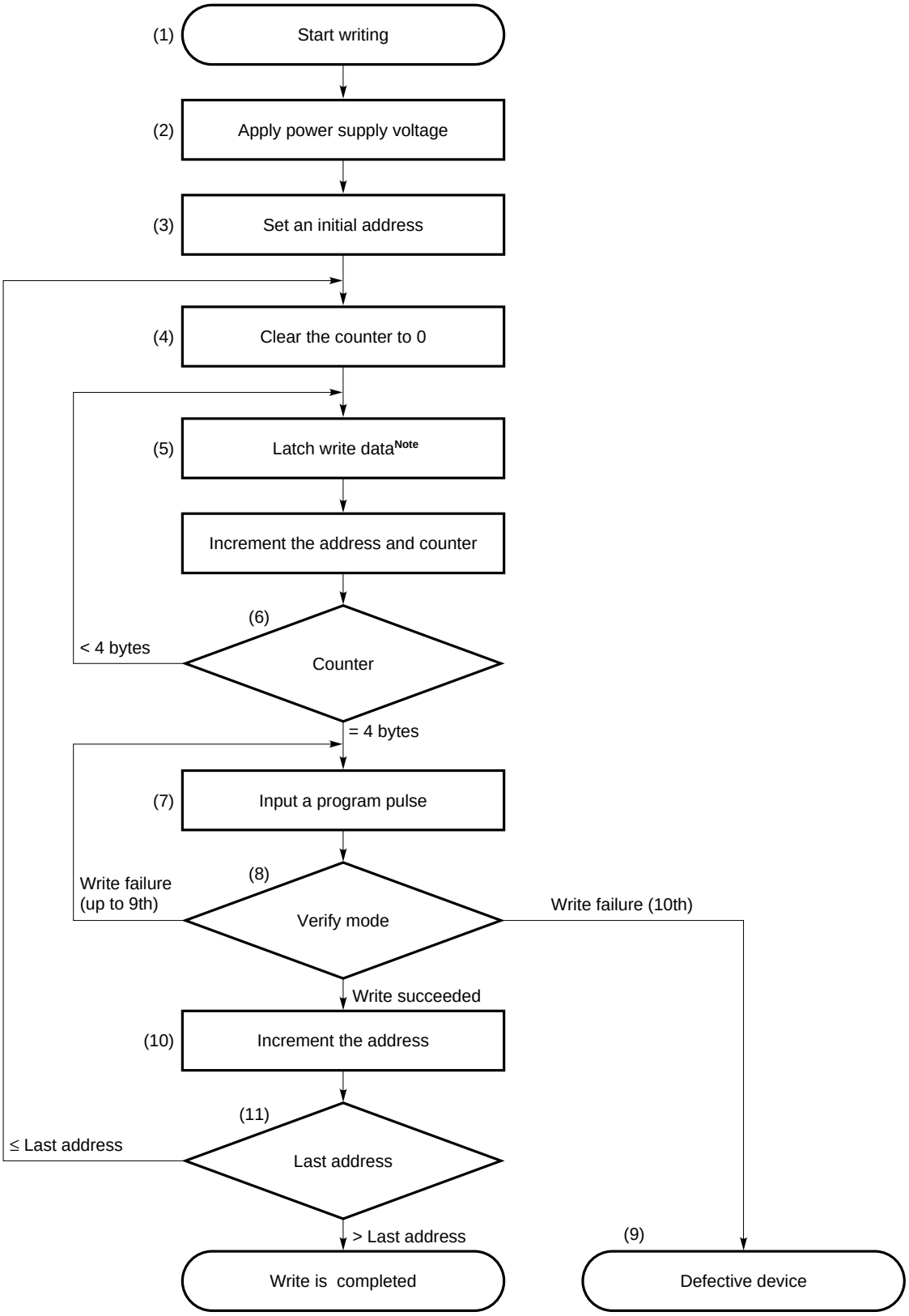
The following is a procedure for writing on PROM. (See **Fig. 4-1**.)

In the page program mode, data is written in units of pages (four bytes). When write data completes midway of a page, latch FFH after the data so that the data fits into pages.

(1) Always set each pin as follows: MODE0/V_{PP} = H and MODE1 = L. Connect unused pins according to PIN CONFIGURATION (2).
(2) Apply +6.5 V to the V_{DD} pin and +12.5 V to the V_{PP} pin.
(3) Input an initial address to the A0 to A16 pins.
(4) Clear the page counter.
(5) Data latch mode. Input write data to the D0 to D7 pins and input an active-low pulse to the $\overline{OE}$ pin. Increment the address and the page counter.
(6) Repeat step (5) for a page (four bytes).
(7) Input a 0.1 ms program pulse (active low) to the $\overline{PGM}$ pin.
(8) Verify mode. Checks if data has been written in PROM.
Apply a low level to the $\overline{CE}$ pin, input an active-low pulse to the $\overline{OE}$ pin, and then read the write data from the D0 to D7 pins. Repeat this for a page (four bytes). When verification completes, apply a high level to the $\overline{CE}$ pin.
    - If data has been written, go to step (10).
    - If not, repeat steps (7) and (8). If no data is written yet after the steps have been repeated 10 times, go to step (9).
(9) Assume the device to be defective and stop write operation.
(10) Increment the address.
(11) Repeat steps (4) to (10) until the address exceeds the last address.

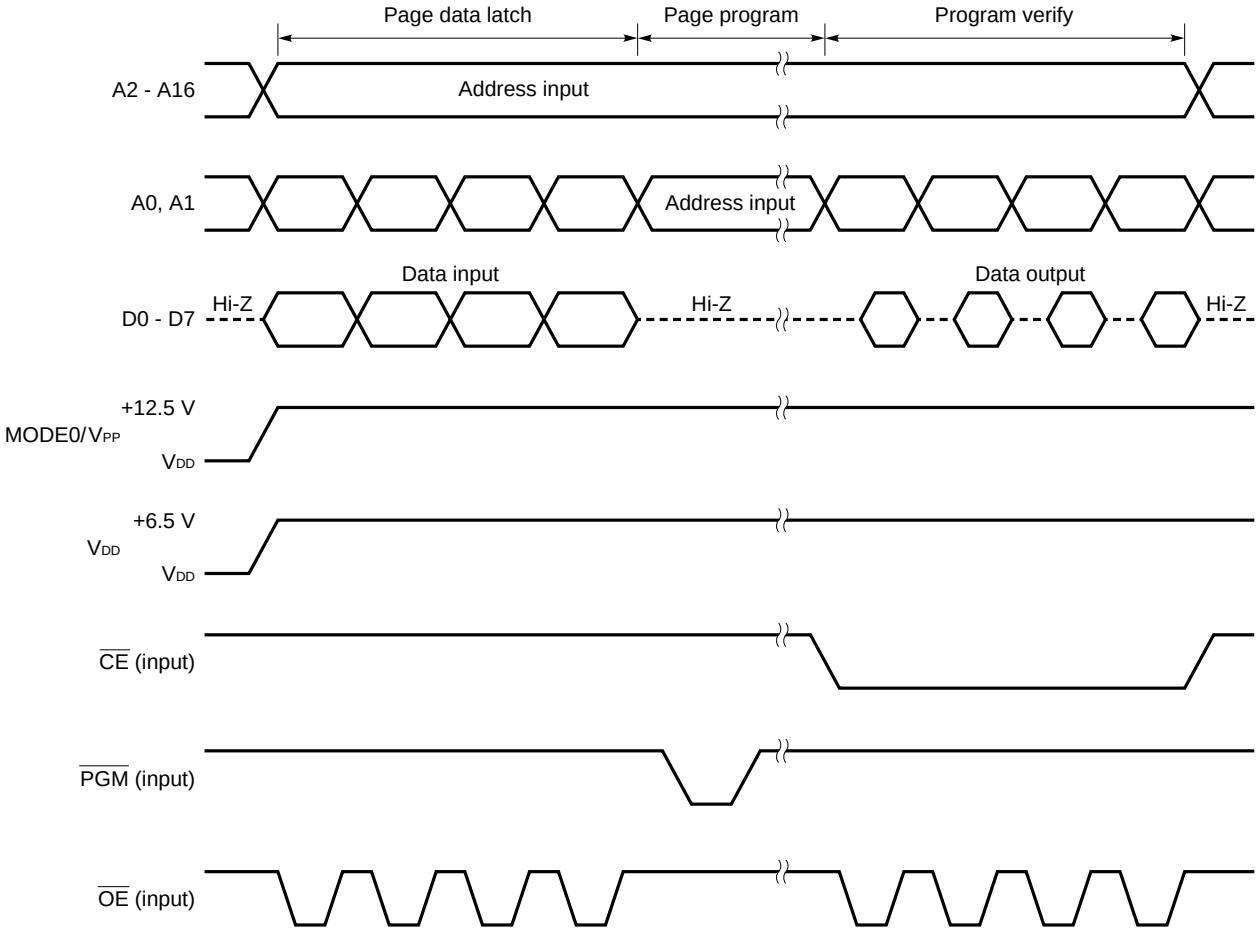
Fig. 4-2 is a timing chart of these steps (2) to (9).

Fig. 4-1 Flowchart of Procedure for Writing (Page Program Mode)



Note If write data does not fill a page, latch FFH for the rest of the page.

Fig. 4-2 PROM Write/Verify Timing Chart (Page Program Mode)



4.3 PROCEDURE FOR WRITING ON PROM (BYTE PROGRAM MODE)

The following is a procedure for writing on PROM. (See **Fig. 4-3**.)

(1) Always set each pin as follows: MODE0/V_{PP} = H and MODE1 = L. Connect unused pins according to PIN CONFIGURATION (2).
(2) Apply +6.5 V to the V_{DD} pin and +12.5 V to the MODE0/V_{PP} pin, and input a low-level signal to the $\overline{CE}$ pin.
(3) Input an initial address to the A0 to A16 pins.
(4) Input write data to the D0 to D7 pins.
(5) Input a 0.1 ms program pulse (active low) to the $\overline{PGM}$ pin.
(6) Verify mode. Checks if data has been written in PROM.
Input an active-low pulse to the $\overline{OE}$ pin and read the write data from the D0 to D7 pins.
- If data has been written, go to step (8).
- If not, repeat steps (4) to (6). If no data is written yet after the steps have been repeated 10 times, go to step (7).

(7) Assume the device to be defective and stop write operation.
(8) Increment the address.
(9) Repeat steps (4) to (8) until the address exceeds the last address.

Fig. 4-4 is a timing chart of these steps (2) to (7).

Fig. 4-3 Flowchart of Procedure for Writing (Byte Program Mode)

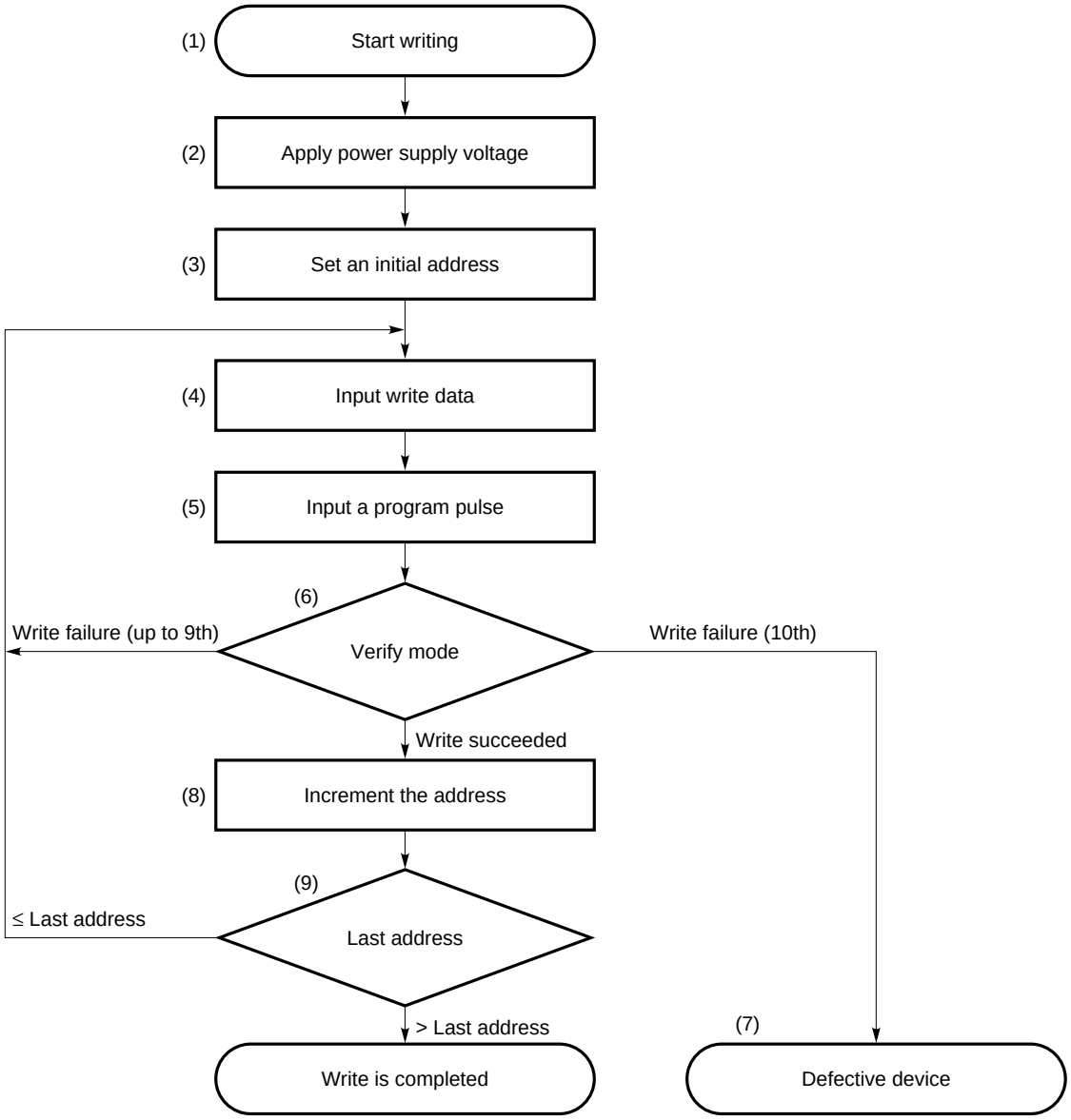
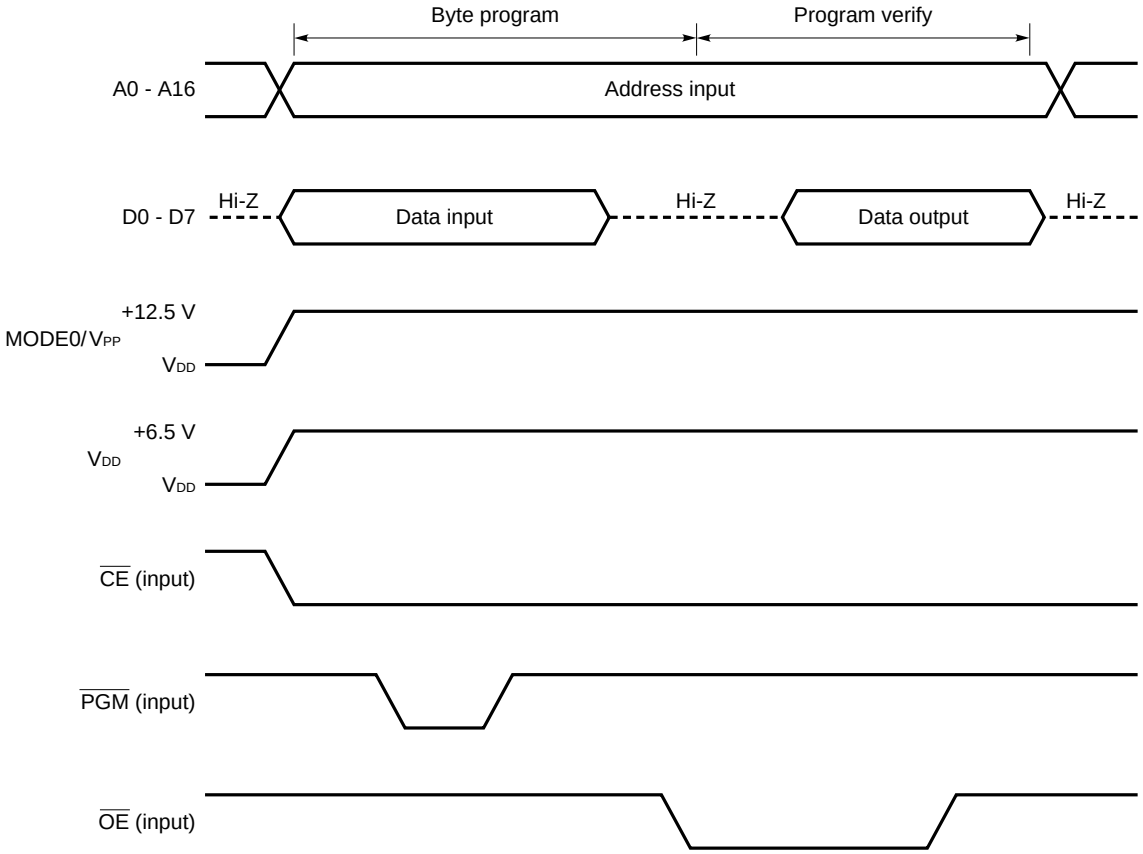


Fig. 4-4 PROM Write/Verify Timing Chart (Byte Program Mode)



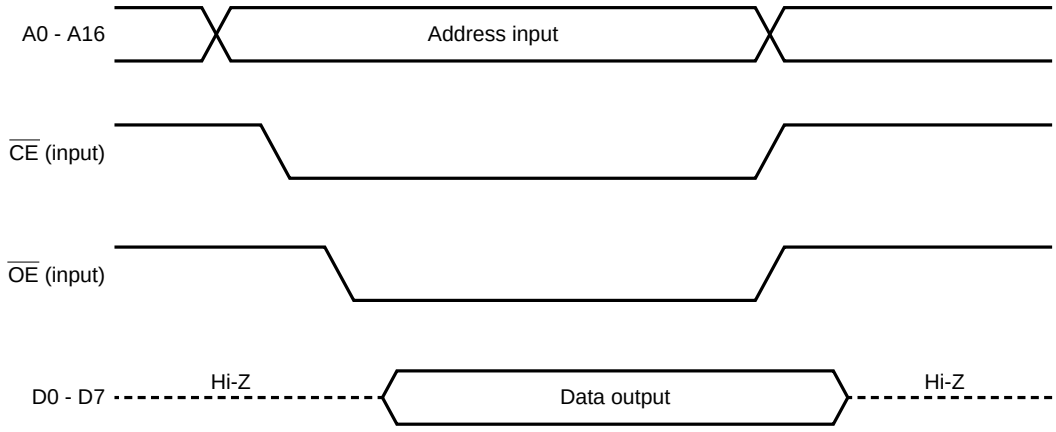
4.4 PROCEDURE FOR READING FROM PROM

The following is a procedure for reading out the contents of PROM to the external data bus (D0 to D7).

(1) Always set each pin as follows: MODE0/V_{PP} = H and MODE1 = L. Connect unused pins according to PIN CONFIGURATION (2).
(2) Apply +5 V to the V_{DD} and MODE0/V_{PP} pins.
(3) Input the address of data to be read into the A0 to A16 pins.
(4) Read mode ($\overline{CE}$ = L, $\overline{OE}$ = L)
(5) Output the data on the D0 to D7 pins.

Fig. 4-5 is a timing chart of these steps (2) to (5).

Fig. 4-5 PROM Read Timing Chart



5. ERASURE CHARACTERISTICS (μPD78P368AKL-S ONLY)

Data written in the μPD78P368AKL-S program memory can be erased (FFH); therefore users can write other data in the memory.

To erase the written data, expose the erasure window to light with a wavelength shorter than approx. 400 nm. Normally, ultraviolet light with a wavelength of 254 nm is employed. The amount of light required to completely erase the data is as follows:

- Intensity of ultraviolet light × erasing time: 15 W•s/cm^2 min.
- Erasing time: 15 to 20 minutes (When using a 12,000 μW/cm^2 ultraviolet lamp. It may, however, take more time due to lamp deterioration, dirt on the erasure window, or the like.)

The ultraviolet lamp should be placed within 2.5 cm from the erasure window during erasure. In addition, if a filter is attached to the ultraviolet lamp, remove the filter before erasure.

6. PROTECTIVE FILM COVERING THE ERASURE WINDOW (μPD78P368AKL-S ONLY)

After the erasure window of the μPD78P368AKL-S has been exposed to sunlight or a fluorescent lamp for a long time, data in EPROM may be erased and the internal circuits may malfunction. To prevent these failures, the erasure window should be covered with a protective film when it is not used for erasure.

EPROM package products with a window are supplied with a NEC-guaranteed protective film when they are delivered.

7. SCREENING ONE-TIME PROM PRODUCTS

NEC cannot execute a complete test of one-time PROM products (μPD78P368AGF-3B9) due to their structure before shipment. It is recommended that you screen (verify) PROM products after writing necessary data into them and storing them at 125 °C for 24 hours.

NEC offers a charged service called QTOP microcomputer service. This service includes writing to one-time PROM, marking, screening, and verification. Ask your sales representative for details.

8. ELECTRICAL SPECIFICATIONS ★

ABSOLUTE MAXIMUM RATINGS (T_A = 25 °C)

Parameter	Symbol	Conditions	Rating	Unit
Power supply voltage	V_{DD}		–0.5 to +7.0	V
	AV_{DD}		–0.5 to V_{DD} + 0.5	V
	V_{PP}		–0.5 to +13.5	V
	AV_{SS}		–0.5 to +0.5	V
Input voltage	V_I	Pins other than P70/ANI0-P77/ANI7	–0.5 to V_{DD} + 0.5	V
Output voltage	V_O		–0.5 to V_{DD} + 0.5	V
Low-level output current	I_{OL}	**Note**	20	mA
		Output pins other than those in the note	4.0	mA
		Total of all output pins	200	mA
High-level output current	I_{OH}	All output pins	–3.0	mA
		Total of all output pins	–25	mA
Analog input voltage	V_{IAN}	P70/ANI0-P77/ANI7 pins	AV_{SS} – 0.5 to AV_{DD} + 0.5	V
A/D converter reference input voltage	AV_{REF}		AV_{SS} – 0.5 to AV_{DD} + 0.5	V
Operating ambient temperature	T_A		–40 to +85	°C
Storage temperature	T_{stg}		–60 to +150	°C

Note P00/RTP0-P03/RTP3, P04/PWM0, P05/TCUD/PWM1, P06/TIUD/TO40, P07/TCLRUD, P10-P17, and P80/TO00-P85/TO05 pins.

Caution Absolute maximum ratings are rated values beyond which some physical damages may be caused to the product; if any of the parameters in the table above exceeds its rated value even for a moment, the quality of the product may deteriorate. Be sure to use the product within the rated values.

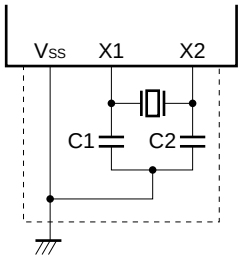
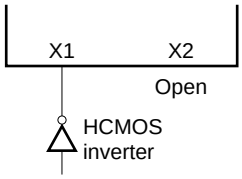
RECOMMENDED OPERATING CONDITIONS

Oscillation frequency	T_A	V_{DD}
3 MHz - f_{XX} - 8 MHz	–40 to +85 °C	+5.0 V ±10 %

CAPACITANCE (T_A = 25 °C, V_{SS} = V_{DD} = 0 V)

Parameter	Symbol	Conditions	Min.	Typ.	Max.	Unit
Input capacitance	C_I	f = 1 MHz			20	pF
Output capacitance	C_O	0 V except measured pins			20	pF
I/O capacitance	C_{IO}				20	pF

OSCILLATOR CHARACTERISTICS (T_A = –40 to +85 °C, V_{DD} = +5 V ±10 %, V_{SS} = 0 V)

Resonator	Recommended circuit	Parameter	Min.	Max.	Unit
Ceramic resonator or crystal		Oscillation frequency (f_{XX})	3	8	MHz
External clock		X1 input frequency (f_X)	3	8	MHz
		X1 rise/fall time (t_{XR}, t_{XF})	0	30	ns
		X1 input high-/low-level width (t_{WXH}, t_{WXL})	40	170	ns

Caution When using system clock oscillation circuits, to reduce the effect of the wiring capacitance, etc, wire the area indicated by dotted-line as follows:

- **Make the wiring as short as possible.**
- **Do not allow the wiring to intersect other signal lines. Keep it away from other lines in which varying high currents flow.**
- **Make sure that the ground point of the oscillation circuit capacitor is always at the same electric potential as V_{SS}. Do not allow the wiring to be grounded to a ground pattern in which very high currents are flowing.**
- **Do not extract signals from the oscillation circuit.**

DC CHARACTERISTICS (T_A = –40 to +85 °C, V_{DD} = +5 V ±10 %, V_{SS} = 0 V)

Parameter	Symbol	Conditions		Min.	Typ.	Max.	Unit
Low-level input voltage	V_{IL1}	**Note 1**		0		0.8	V
	V_{IL2}	**Note 2**		0		$0.2V_{DD}$	V
High-level input voltage	V_{IH1}	**Note 1**		2.2			V
	V_{IH2}	**Note 2**		$0.8V_{DD}$			V
Low-level output voltage	V_{OL1}	**Note 3**	I_{OL} = 2.0 mA			0.45	V
	V_{OL2}	**Note 4**	I_{OL} = 15 mA			1.5	V
	V_{OL3}	**Note 5**	I_{OL} = 10 mA			1.5	V
High-level output voltage	V_{OH}	I_{OH} = –400 μA		V_{DD} – 1.0			V
Input leakage current	I_{LI}	0 V - V_I - V_{DD}, AV_{DD} = V_{DD}				±10	μA
Output leakage current	I_{LO}	0 V - V_O - V_{DD}, AV_{DD} = V_{DD}				±10	μA
V_{DD} supply current	I_{DD1}	Operating mode			70	120	mA
	I_{DD2}	HALT mode			45	70	mA
Data retention voltage	V_{DDDR}	STOP mode		2.5			V
Data retention current	I_{DDDR}	STOP mode	V_{DDDR} = 2.5 V		2	10	μA
			V_{DDDR} = 5.0 V ±10 %		10	50	μA
Pull-up resistance	R_L	V_I = 0 V		15	60	150	K ý

Notes 1. Pins other than those specified in **Note 2**.

2. $\overline{\text{RESET}}$, X1, X2, P20/NMI, P21/INTP0, P22/INTP1, P23/INTP2, P24/INTP3/TI, P25/INTP4, P32/SO/SB0, P33/SI/SB1 and P34/$\overline{\text{SCK}}$ pins.

3. Pins other than those specified in **Notes 4 and 5**.

4. P80/TO00-P85/TO05 pins (When I_{OL} = 15 mA is in operation, up to three pins can be ON simultaneously.)

5. P00/RTP0-P03/RTP3, P04/PWM0, P05/TCUD/PWM1, P06/TIUD/TO40 and P07/TCLRUD pins (When I_{OL} = 10 mA is in operation, up to four pins can be ON simultaneously.) as well as P10-P17 pins (When I_{OL} = 10 mA is in operation, up to four pins can be ON simultaneously.).

Caution When the P80-P85, P00-P07, and P10-P17 pins are not used under the conditions specified in Notes 4 and 5, they have the same characteristics as in Note 3.

AC CHARACTERISTICS (T_A = –40 to +85 °C, V_{DD} = +5 V ±10 %, V_{SS} = 0 V, C_L = 100 pF, f_{XX} = 8 MHz)

Read/Write Operation (when general-purpose memory is connected)

Parameter	Symbol	Conditions	Min.	Max.	Unit
System clock cycle time	t_{CYK}		62.5	166.7	ns
Address setup time (vs. ASTB ↓)	t_{SAST}		7		ns
Address hold time (vs. ASTB ↓)	t_{HSTA}		11		ns
$\overline{RD}$ ↓ → address float time	t_{FRA}			24	ns
Address → data input time	t_{DAID}			100	ns
$\overline{RD}$ ↓ → data input time	t_{DRID}			49	ns
ASTB ↓ → $\overline{RD}$ ↓ delay time	t_{DSTR}		15		ns
Data hold time (vs. $\overline{RD}$ ∞)	t_{HRID}		0		ns
$\overline{RD}$ ∞ → address active time	t_{DRA}		17		ns
$\overline{RD}$ low-level width	t_{WRL}		63		ns
ASTB high-level width	t_{WSTH}		14		ns
$\overline{WR}$ ↓ → data output time	t_{DWOD}			21	ns
ASTB ↓ → $\overline{WR}$ ↓ delay time	t_{DSTW}		15		ns
$\overline{WR}$ ∞ → ASTB ∞ delay time	t_{DWST}		78		ns
Data setup time (vs. $\overline{WR}$ ∞)	t_{SODW}		57		ns
Data hold time (vs. $\overline{WR}$ ∞)	t_{HWOD}		8		ns
$\overline{WR}$ low-level width	t_{WWL}		63		ns

t_{CYK}-dependent Bus Timing Definition

Parameter	Arithmetic expression	Min./Max.	Unit
t_{SAST}	(0.5 + a) T – 24	Min.	ns
t_{HSTA}	0.5T – 20	Min.	ns
t_{WSTH}	(0.5 + a) T – 17	Min.	ns
t_{DSTR}	0.5T – 16	Min.	ns
t_{WRL}	(1.5 + n) T – 30	Min.	ns
t_{DAID}	(2.5 + a + n) T – 56	Max.	ns
t_{DRID}	(1.5 + n) T – 44	Max.	ns
t_{DRA}	0.5T – 14	Min.	ns
t_{DSTW}	0.5T – 16	Min.	ns
t_{DWST}	1.5T – 15	Min.	ns
t_{WWL}	(1.5 + n) T – 30	Min.	ns
t_{DWOD}	0.5T – 10	Max.	ns
t_{SODW}	(1 + n) T – 5	Min.	ns

Remarks 1. T = t_{CYK} = 1/f_{CLK} (f_{CLK} refers to the internal system clock frequency.)

2. a becomes 1 when the address wait is inserted. Otherwise, it becomes 0.

3. n refers to the number of wait cycles that is inserted by specifying the PWC register.

4. Only the bus timings indicated in this table depend on t_{CYK}.

SERIAL OPERATION (T_A = –40 to +85 °C, V_{DD} = +5 V ±10 %, V_{SS} = 0 V)

Parameter	Symbol	Conditions		Min.	Max.	Unit
Serial clock cycle time	t_{CYSK}	$\overline{SCK}$ output	Internal 8 dividing	500		ns
		$\overline{SCK}$ input	External clock	500		ns
Serial clock low-level width	t_{WSKL}	$\overline{SCK}$ output	Internal 8 dividing	210		ns
		$\overline{SCK}$ input	External clock	210		ns
Serial clock high-level width	t_{WSKH}	$\overline{SCK}$ output	Internal 8 dividing	210		ns
		$\overline{SCK}$ input	External clock	210		ns
SI setup time (vs. $\overline{SCK}$ ∞)	t_{SRXSK}			80		ns
SI hold time (vs. $\overline{SCK}$ ∞)	t_{HSKRX}			80		ns
$\overline{SCK}$ ↓ → SO delay time	t_{DSKTX}	R = 1 ký, C = 100 pF			210	ns

UP/DOWN COUNTER OPERATION (T_A = –40 to +85 °C, V_{DD} = +5 V ±10 %, V_{SS} = 0 V)

Parameter	Symbol	Conditions	Min.	Max.	Unit
TIUD high-/low-level width	t_{WTIUH}, t_{WTIUL}	Other than mode 4	2T		ns
		Mode 4	4T		ns
TCUD high-/low-level width	t_{WTCUH}, t_{WTCUL}	Other than mode 4	2T		ns
		Mode 4	4T		ns
TCLRUD high-/low-level width	t_{WCLUH}, t_{WCLUL}		2T		ns
TCUD setup time (vs. TIUD ∞)	t_{STCU}	Mode 3	T		ns
TCUD hold time (vs. TIUD ∞)	t_{HTCU}	Mode 3	T		ns
TIUD setup time (vs. TCUD)	t_{S4TIU}	Mode 4	2T		ns
TIUD hold time (vs. TCUD)	t_{H4TIU}	Mode 4	2T		ns
TIUD & TCUD cycle time	t_{CYC}	Other than mode 4		4	MHz
	t_{CYC4}	Mode 4		2	MHz

Remark T = t_{CYK} = 1/f_{CLK} (f_{CLK} refers to the internal system clock frequency.)

OTHER OPERATIONS (T_A = –40 to +85 °C, V_{DD} = +5 V ±10 %, V_{SS} = 0 V)

Parameter	Symbol	Conditions	Min.	Max.	Unit
NMI high-/low-level width	t_{WNIH}, t_{WNIL}		2		μs
$\overline{\text{RESET}}$ high-/low-level width	t_{WRSH}, t_{WRSL}		1.5		μs
INTP0 high-/low-level width	t_{WI0H}, t_{WI0L}	Ts = T	250		ns
		Ts = 4T	1.0		μs
		Ts = 8T	2.0		μs
		Ts = 16T	4.0		μs
INTP1 high-/low-level width	t_{WI1H}, t_{WI1L}	Ts = T	250		ns
		Ts = 4T	1.0		μs
		Ts = 8T	2.0		μs
		Ts = 16T	4.0		μs
INTP2 high-/low-level width	t_{WI2H}, t_{WI2L}	Ts = T	250		ns
		Ts = 4T	1.0		μs
INTP3(TI) high-/low-level width	t_{WI3H}, t_{WI3L}	Ts = T	250		ns
		Ts = 4T	1.0		μs
		Ts = 8T	2.0		μs
		Ts = 16T	4.0		μs
		Ts = 64T	16.0		μs
		Ts = 128T	32.0		μs
		Ts = 256T	64.0		μs
INTP4 high-/low-level width	t_{WI4H}, t_{WI4L}	Ts = T	250		ns
		Ts = 4T	1.0		μs
		Ts = 8T	2.0		μs
		Ts = 16T	4.0		μs

Remarks 1. T = t_{CYK} = 1/f_{CLK} (f_{CLK} refers to the internal system clock frequency.)

2. Ts refers to the input sampling frequency. INTP0-INTP4 can be selected to programmable.

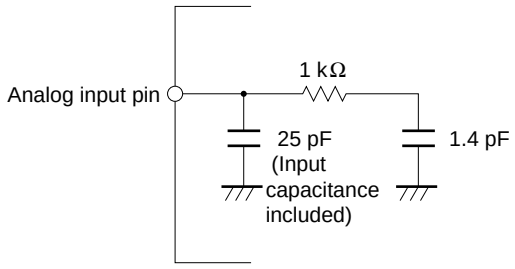
A/D CONVERTER CHARACTERISTICS (T_A = –40 to +85 °C, V_{DD} = +5 V ±10 %, V_{SS} = AV_{SS} = 0 V, V_{DD} – 0.5 V - AV_{DD} - V_{DD})

Parameter	Symbol	Conditions		Min.	Typ.	Max.	Unit
Resolution				10			bit
Total error[Note 1]		4.5 V - AV_{REF} - AV_{DD}				±0.4	%FSR
		3.4 V - AV_{REF} - AV_{DD}				±0.7	%FSR
Quantization error						±1/2	LSB
Conversion time	t_{CONV}	62.5 ns - t_{CYK} < 80 ns		208			t_{CYK}
		80 ns - t_{CYK} - 166.6 ns		169			t_{CYK}
Sampling time	t_{SAMP}	62.5 ns - t_{CYK} < 80 ns		8			t_{CYK}
		80 ns - t_{CYK} - 166.6 ns		6			t_{CYK}
Zero-scale error[Note 1]		4.5 V - AV_{REF} - AV_{DD}			±1.5	±2.5	LSB
		3.4 V - AV_{REF} - AV_{DD}			±1.5	±4.5	LSB
Full-scale error[Note 1]		4.5 V - AV_{REF} - AV_{DD}			±1.5	±2.5	LSB
		3.4 V - AV_{REF} - AV_{DD}			±1.5	±4.5	LSB
Nonlinearity error[Note 1]		4.5 V - AV_{REF} - AV_{DD}			±1.5	±2.5	LSB
		3.4 V - AV_{REF} - AV_{DD}			±1.5	±4.5	LSB
Analog input voltage[Note 2]	V_{IAN}			–0.3		AV_{REF} + 0.3	V
Analog input impedance	R_{AN}	When not sampling			10		MΩ
		When sampling			Note 3		
Reference voltage	AV_{REF}			3.4		AV_{DD}	V
AV_{REF1} current	AI_{REF}				1.0	3.0	mA
AV_{DD} supply current	AI_{DD}	Operating mode			2.0	6.0	mA
A/D converter data retention current	AI_{DDDR}	STOP mode	AV_{DDDR} = 2.5 V		2	10	μA
			AV_{DDDR} = 5 V ±10 %		10	50	μA

Notes 1. The quantization error is excluded.

2. When –0.3 V - V_{IAN} - 0 V, the conversion result becomes 000H.
When 0 V < V_{IAN} < AV_{REF}, the conversion is performed with the 10-bit resolution.
When AV_{REF} - V_{IAN} - AV_{REF} + 0.3 V, the conversion result becomes 3FFH.

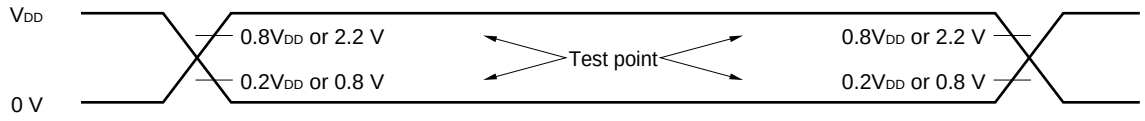
3. The analog input impedance at the time of sampling is the same as the equivalent circuit shown below.
(The values in the diagram are TYP. values; they are not guaranteed values.)



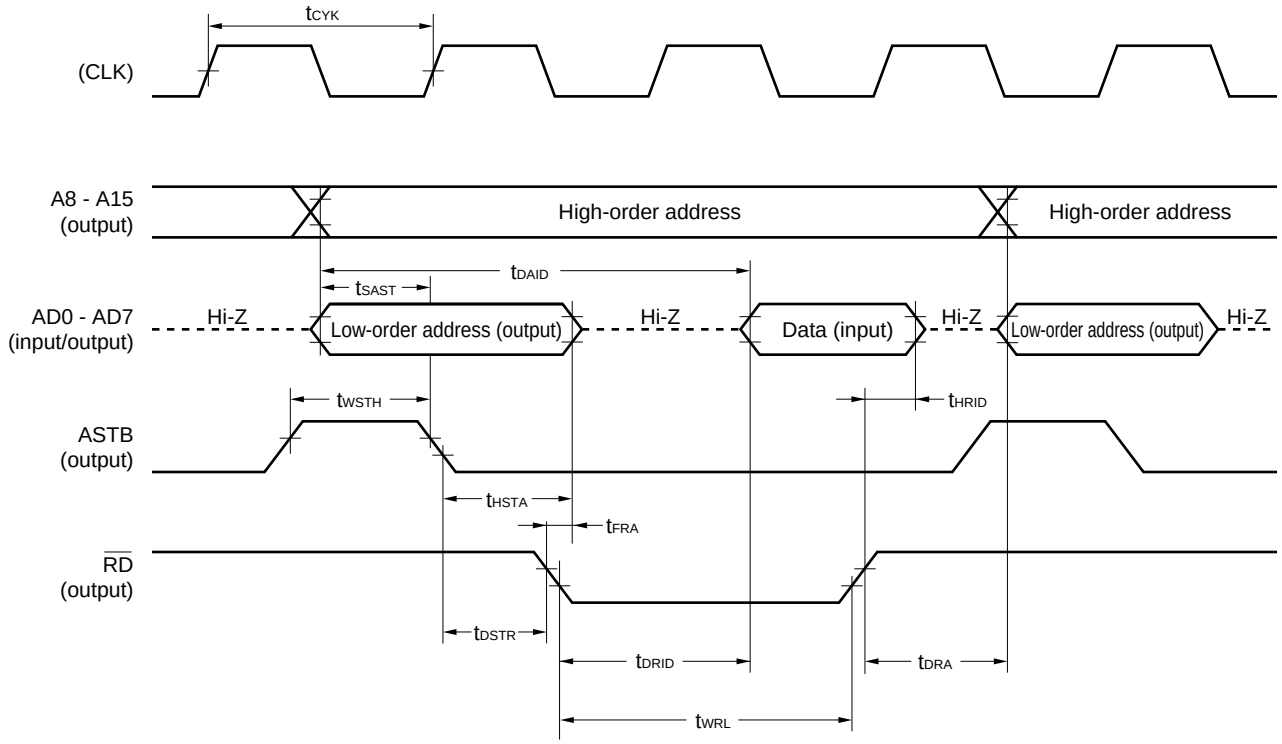
Cautions 1. When using the P70/ANI0-P77/ANI7 pins for both digital and analog inputs, the previously described characteristics are not guaranteed. Therefore, ensure that all of the eight P70/ANI0-P77/ANI7 pins are used either for analog input or digital input.

2. When using the P70/ANI0-P77/ANI7 pins as digital input, make sure to set that $AV_{DD} = V_{DD}$, and $AV_{SS} = V_{SS}$.

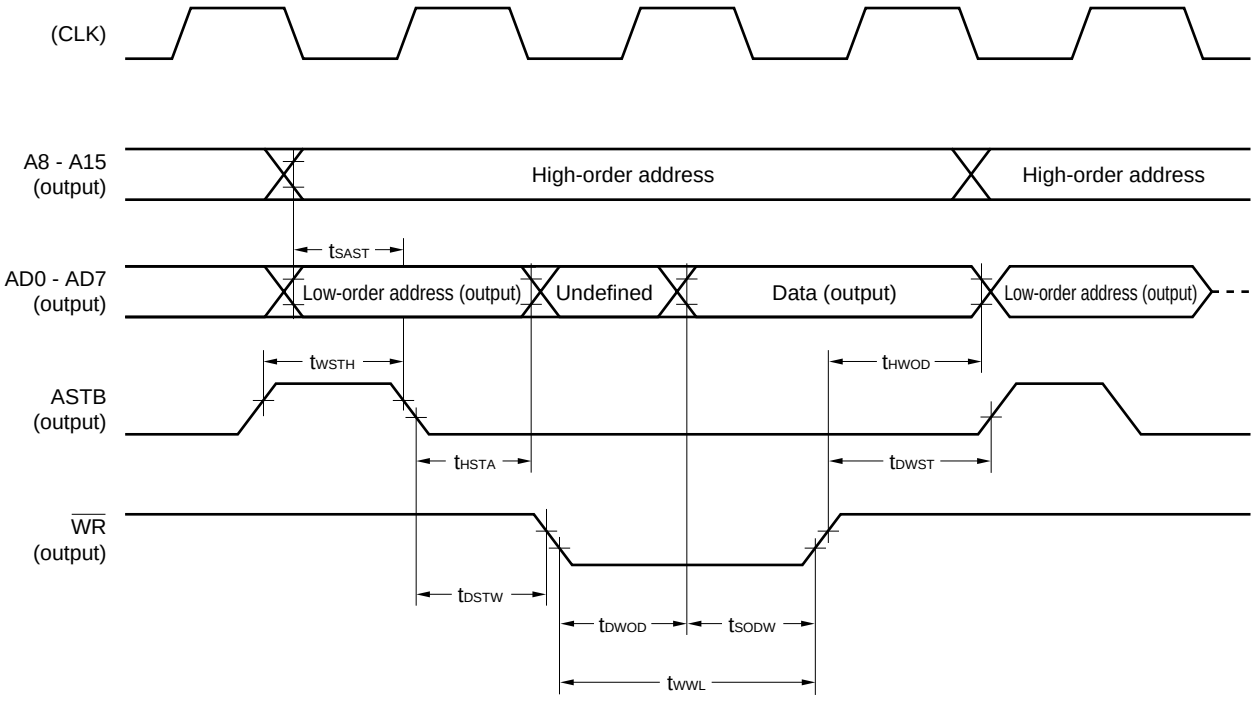
AC Timing Test Point



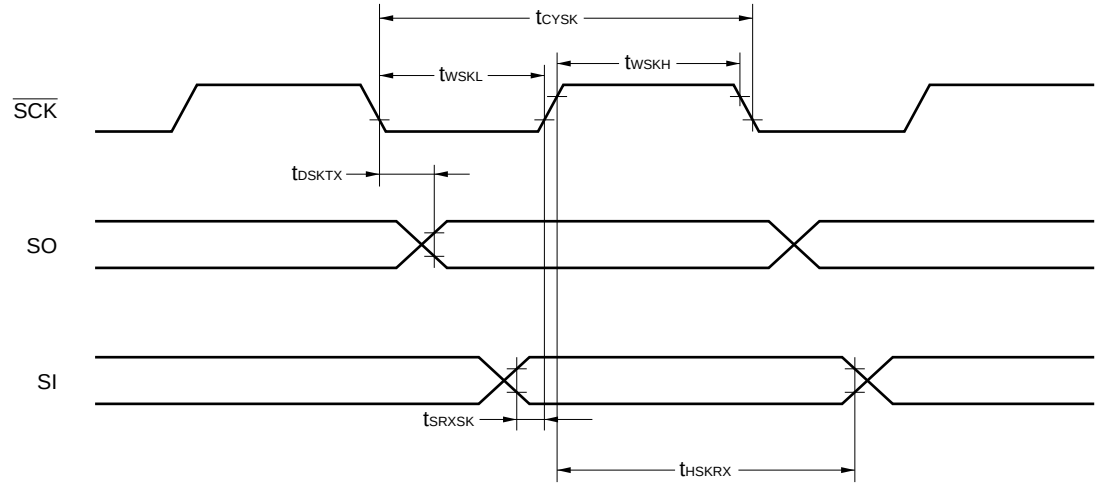
Read Operation



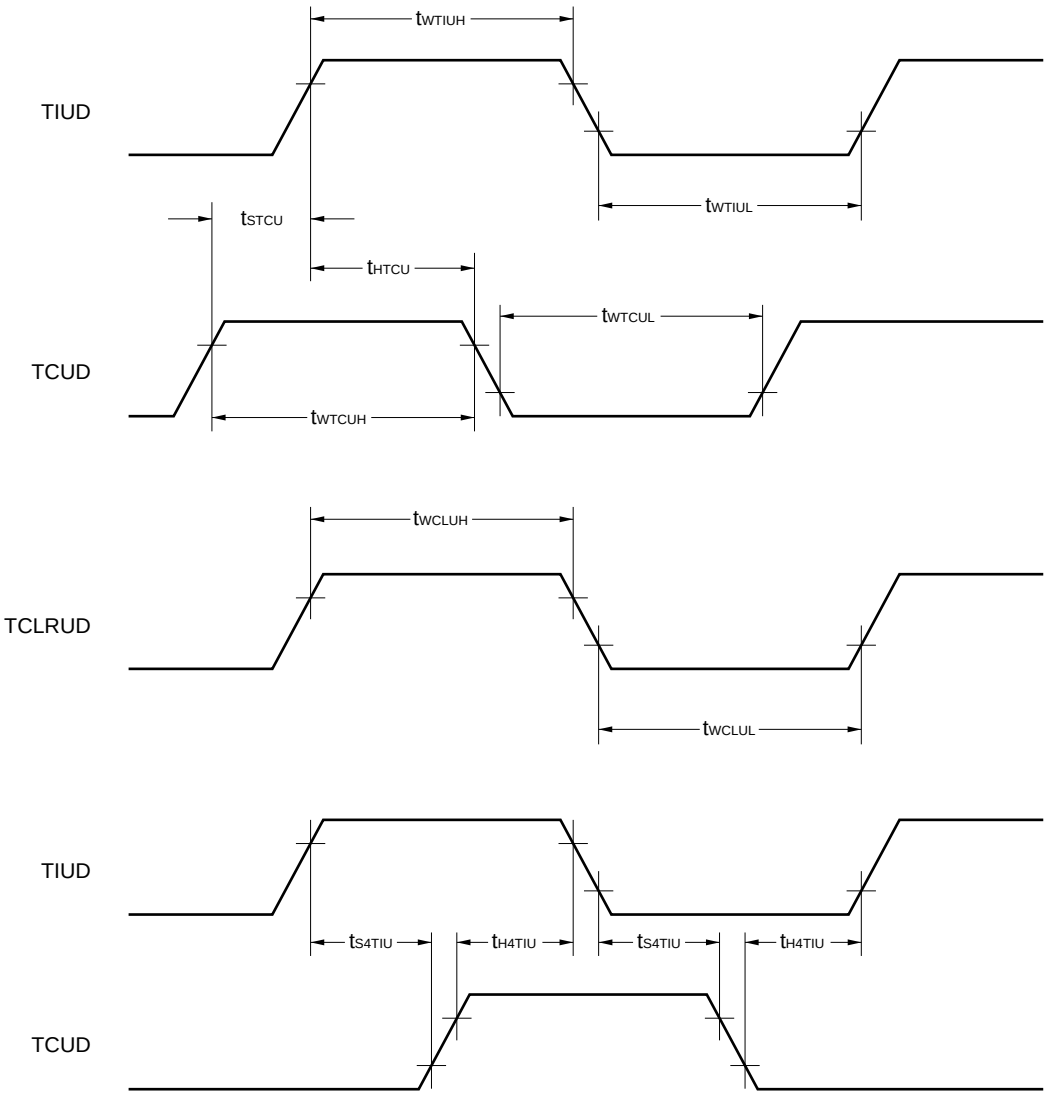
Write Operation



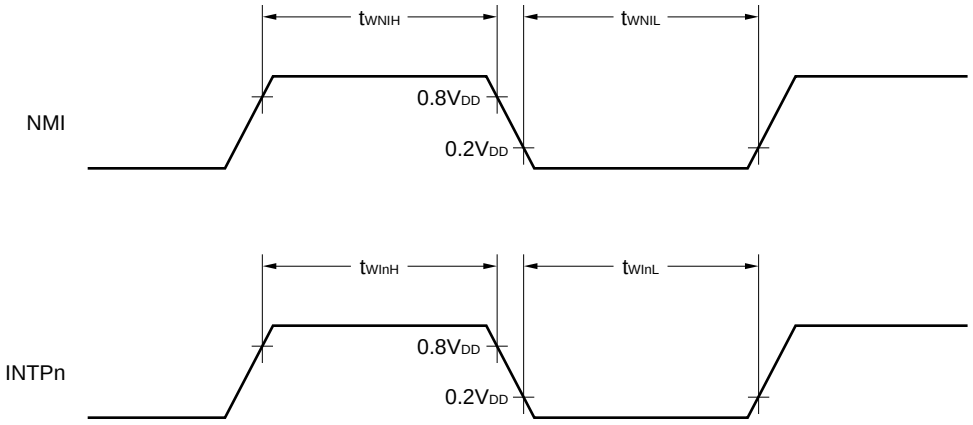
Serial Operation



Up/Down Counter (Timer 4) Input Timing

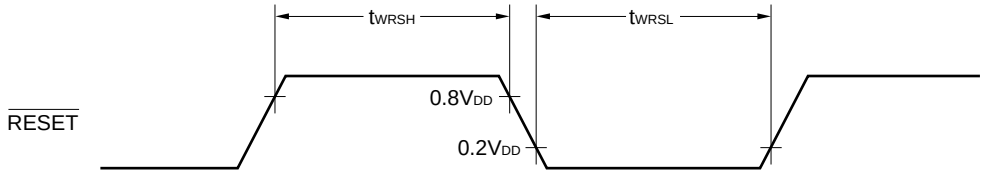


Interrupt Input Timing



Remark n = 0 – 4

Reset Input Timing



DC PROGRAMMING CHARACTERISTICS (T_A = 25 ±5 °C, V_{SS} = 0 V)

Parameter	Symbol	Symbol[Note 1]	Conditions	Min.	Typ.	Max.	Unit
High-level input voltage	V_{IH}	V_{IH}		2.4		V_{DDP} + 0.3	V
Low-level input voltage	V_{IL}	V_{IL}		–0.3		0.8	V
Input leakage current	I_{LIP}	I_{LI}	0 - V_I - V_{DDP}[Note 2]			±10	μA
High-level output voltage	V_{OH}	V_{OH}	I_{OH} = –400 μA	2.4			V
Low-level output voltage	V_{OL}	V_{OL}	I_{OL} = 2.1 mA			0.45	V
Output leakage current	I_{LO}	–	0 - V_O - V_{DDP}, $\overline{OE}$ = V_{IH}			±10	μA
V_{DDP} supply voltage	V_{DDP}	V_{CC}	Program memory write mode	6.25	6.5	6.75	V
			Program memory read mode	4.5	5.0	5.5	V
V_{PP} supply voltage	V_{PP}	V_{PP}	Program memory write mode	12.2	12.5	12.8	V
			Program memory read mode	V_{DD} – 0.6	V_{DD}	V_{DD} + 0.6	V
V_{DDP} supply current	I_{DD}	I_{DD}	Program memory write mode			50	mA
			Program memory read mode			50	mA
V_{PP} supply current	I_{PP}	I_{PP}	Program memory write mode			50	mA
			Program memory read mode			100	μA

Notes 1. Symbols for the corresponding μPD27C1001A

2. The V_{DDP} represents the V_{DD} pin as viewed in the programming mode.

AC PROGRAMMING CHARACTERISTICS (T_A = 25 ±5 °C, V_{SS} = 0 V)

PROM Write Mode (Page Program Mode)

Parameter	Symbol[Note 1]	Conditions	Min.	Typ.	Max.	Unit
Address set up time	t_{AS}		2			μs
$\overline{CE}$ set time	t_{CES}		2			μs
Input data setup time	t_{DS}		2			μs
Address hold time	t_{AH}		2			μs
	t_{AHL}		2			μs
	t_{AHV}		0			μs
Input data hold time	t_{DH}		2			μs
Output data hold time	t_{DF}		0		250	ns
V_{PP} setup time	t_{VPS}		1			ms
V_{DDP} setup time	t_{VDS}[Note 2]		1			ms
Initial program pulse width	t_{PW}		0.095		0.105	ms
$\overline{OE}$ set time	t_{OES}		2			μs
Valid data delay time from $\overline{OE}$	t_{OE}				1.0	μs
$\overline{OE}$ pulse width in the data latch	t_{LW}		1			μs
$\overline{PGM}$ setup time	t_{PGMS}		2			μs
$\overline{CE}$ hold time	t_{CEH}		2			μs
$\overline{OE}$ hold time	t_{OEH}		2			μs

Notes 1. These symbols (except t_{VDS}) correspond to those of the μPD27C1001A.

2. For μPD27C1001A, read t_{VDS} as t_{VCS}.

PROM Write Mode (Byte Program Mode)

Parameter	Symbol[Note 1]	Conditions	Min.	Typ.	Max.	Unit
Address set up time	t_{AS}		2			μs
$\overline{CE}$ set time	t_{CES}		2			μs
Input data setup time	t_{DS}		2			μs
Address hold time	t_{AH}		2			μs
Input data hold time	t_{DH}		2			μs
Output data hold time	t_{DF}		0		250	ns
V_{PP} setup time	t_{VPS}		1			ms
V_{DDP} setup time	t_{VDS}[Note 2]		1			ms
Initial program pulse width	t_{PW}		0.095		0.105	ms
$\overline{OE}$ set time	t_{OES}		2			μs
Valid data delay time from $\overline{OE}$	t_{OE}				1.0	μs

Notes 1. These symbols (except t_{VDS}) correspond to those of the μPD27C1001A.

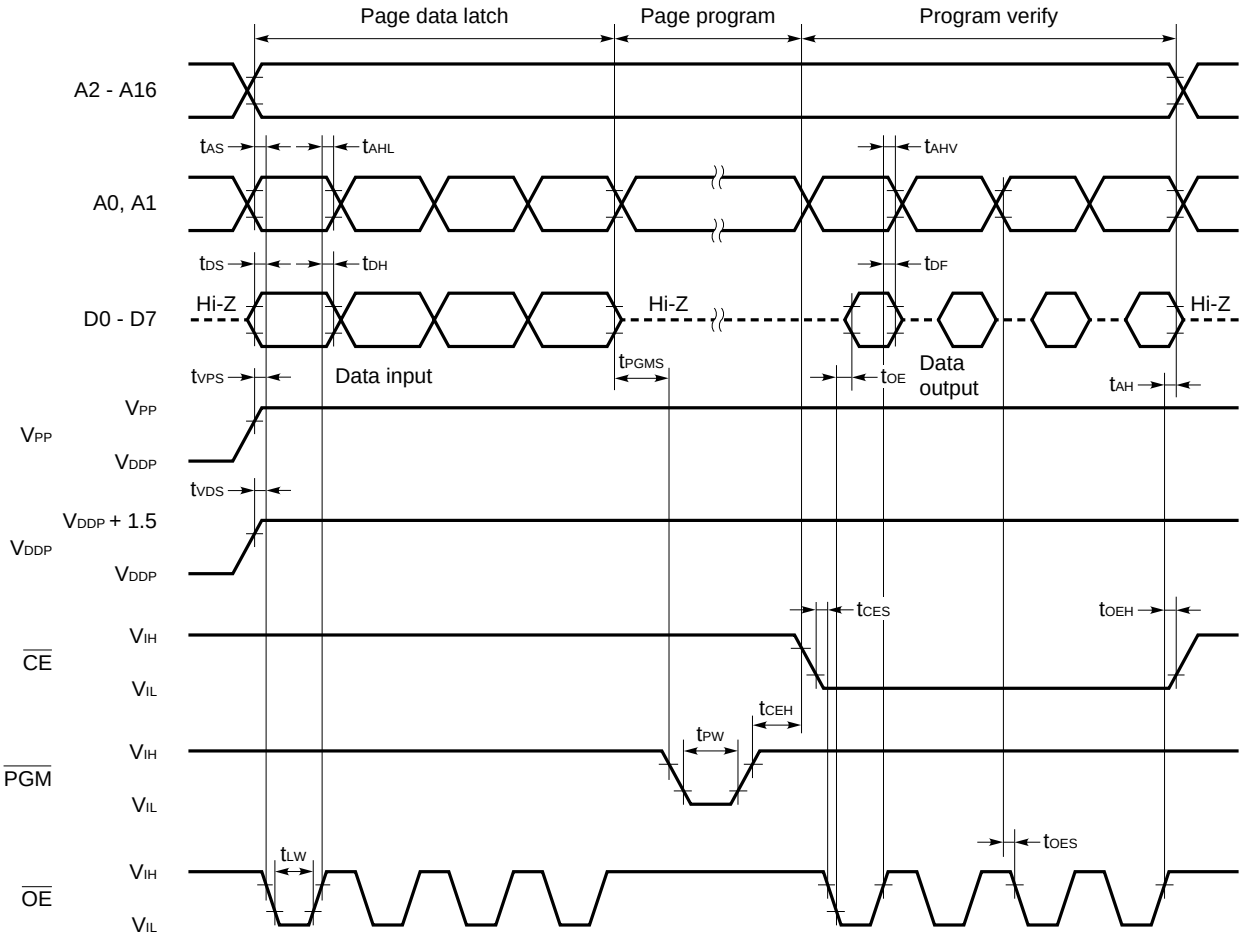
2. For μPD27C1001A, read t_{VDS} as t_{VCS}.

PROM Read Mode

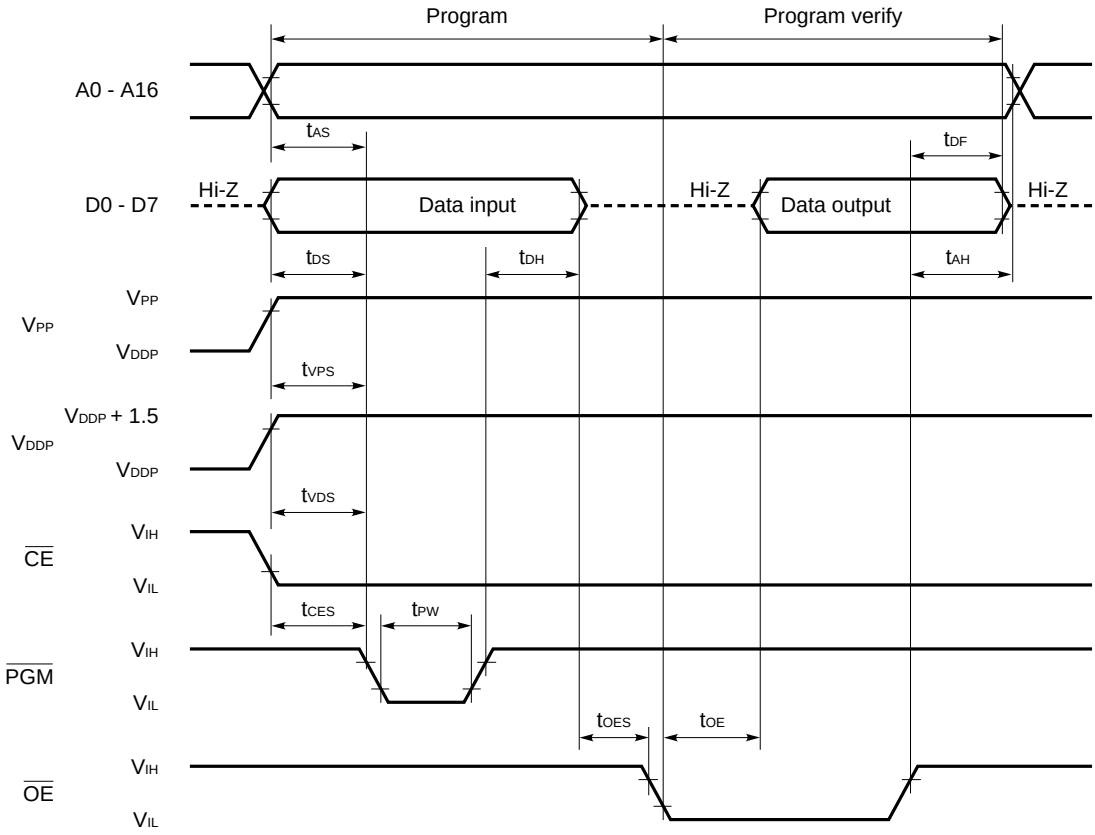
Parameter	Symbol[Note]	Conditions	Min.	Typ.	Max.	Unit
Data output time from address	t_{ACC}	$\overline{CE} = \overline{OE} = V_{IL}$			1.0	μs
$\overline{CE} \downarrow \rightarrow$ data output time	t_{CE}	$\overline{OE} = V_{IL}$			1.0	μs
$\overline{OE} \downarrow \rightarrow$ data output time	t_{OE}	$\overline{CE} = V_{IL}$			1.0	μs
Data hold time to $\overline{OE} \infty$	t_{DF}	$\overline{CE} = V_{IL}$	0		250	ns
Data hold time to address	t_{OH}	$\overline{CE} = \overline{OE} = V_{IL}$	0			ns

Note These symbols correspond to those of the μPD27C1001A.

PROM Write Mode Timing (Page Program Mode)



PROM Write Mode Timing (Byte Program Mode)

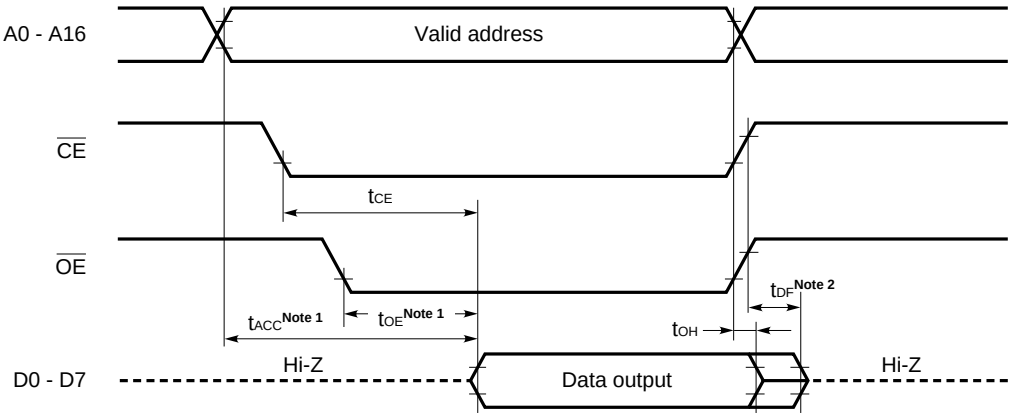


Cautions 1. V_{DDP} must be applied before V_{PP}, and must be cut after V_{PP}.

2. V_{PP} including overshoot must not exceed +13.5 V.

3. Plugging in or out the board with the V_{PP} pin supplied with +12.5 V may adversely affect its reliability.

PROM Read Mode Timing

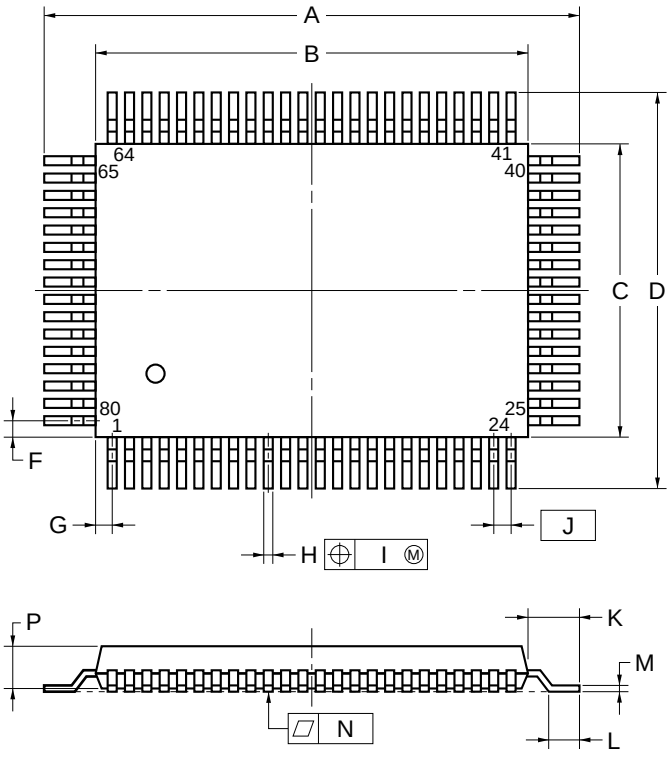


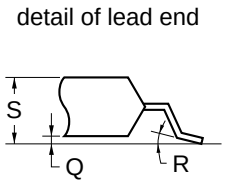
Notes 1. For reading within t_{ACC}, the delay of the $\overline{OE}$ input from falling edge of $\overline{CE}$ must be within $t_{ACC} - t_{OE}$.

2. t_{DF} is the time measured from when either $\overline{OE}$ or $\overline{CE}$ reaches V_{IH}, whichever is faster.

9. PACKAGE DRAWINGS

80 PIN PLASTIC QFP (14×20)





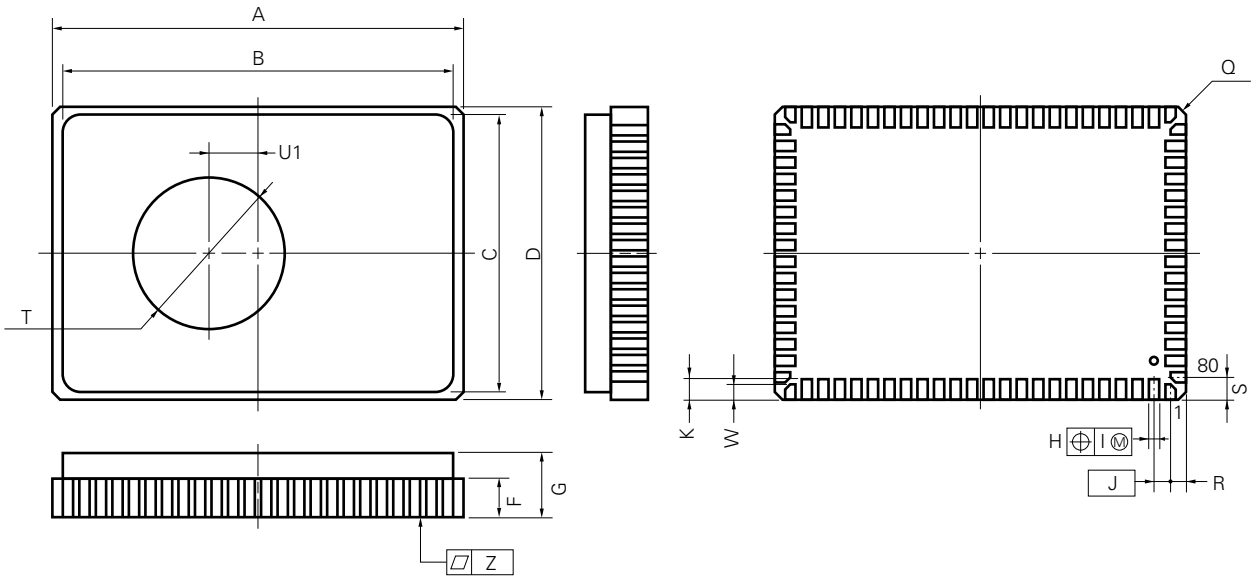
NOTE

Each lead centerline is located within 0.15 mm (0.006 inch) of its true position (T.P.) at maximum material condition.

ITEM	MILLIMETERS	INCHES
A	23.6±0.4	0.929±0.016
B	20.0±0.2	$0.795^{+0.009}_{-0.008}$
C	14.0±0.2	$0.551^{+0.009}_{-0.008}$
D	17.6±0.4	0.693±0.016
F	1.0	0.039
G	0.8	0.031
H	0.35±0.10	$0.014^{+0.004}_{-0.005}$
I	0.15	0.006
J	0.8 (T.P.)	0.031 (T.P.)
K	1.8±0.2	$0.071^{+0.008}_{-0.009}$
L	0.8±0.2	$0.031^{+0.009}_{-0.008}$
M	$0.15^{+0.10}_{-0.05}$	$0.006^{+0.004}_{-0.003}$
N	0.10	0.004
P	2.7	0.106
Q	0.1±0.1	0.004±0.004
R	5°±5°	5°±5°
S	3.0 MAX.	0.119 MAX.

P80GF-80-3B9-3

80 PIN CERAMIC WQFN



X80KW-80A1

ITEM	MILLIMETERS	INCHES
A	20.0±0.25	$0.787^{+0.011}_{-0.010}$
B	19.0	0.748
C	13.4	0.528
D	14.2±0.2	0.559±0.008
F	1.84	0.072
G	3.56MAX.	0.141MAX.
H	0.51±0.1	0.02±0.004
I	0.08	0.003
J	0.8 (T.P.)	0.031 (T.P.)
K	1.0±0.15	$0.039^{+0.007}_{-0.006}$
Q	C0.3	C0.012
R	0.8	0.031
S	1.1	0.043
T	ϕ7.62	ϕ0.3
U1	2.6	0.102
W	0.75±0.15	$0.03^{+0.006}_{-0.007}$
Z	0.10	0.004

NOTE

Each lead centerline is located within 0.08 mm (0.003 inch) of its true position (T.P.) at maximum material condition.

10. RECOMMENDED SOLDERING CONDITIONS ★

These products should be soldered and mounted under the conditions recommended below.

For details of recommended soldering conditions, refer to the information document *Semiconductor Device Mounting Technology Manual* (C10535J).

For soldering methods and conditions other than those recommended, please contact your NEC sales representative.

Table 10-1. Surface Mount Type Soldering Conditions

μPD78P368AGF-3B9: 80-Pin Plastic QFP (14 × 20 mm)

Soldering method	Soldering conditions	Recommended condition symbol
Infrared reflow	Package peak temperature: 235 °C, Duration: 30 sec. max. (210 °C or above) Number of times: 2 max. Exposure limit: 7 days[Note] (20 hours of pre-baking is required at 125 °C afterward) <Caution> Non-heat-resistant trays, such as magazine and taping trays, cannot be baked before unpacking.	IR35-207-2
VPS	Package peak temperature: 215 °C, Duration: 40 sec. max. (200 °C or above) Number of times: 2 max. Exposure limit: 7 days[Note] (20 hours of pre-baking is required at 125 °C afterward) <Caution> Non-heat-resistant trays, such as magazine and taping trays, cannot be baked before unpacking.	VP15-207-2
Wave soldering	Solder bath temperature: 260 °C or less, Time: 10 sec. max., Number of times: 1, Pre-heating temperature: 120 °C max. (Package surface temperature) Exposure limit: 7 days[Note] (20 hours of pre-baking is required at 125 °C afterward)	WS60-207-1
Partial heating	Pin temperature: 300 °C or less Duration: 3 sec. max. (per side of device)	–

Note Maximum number of days during which the product can be stored at a temperature of 25 °C and a relative humidity of 65 % or less after dry-pack package is opened.

Caution Use of more than one soldering method should be avoided (except in the case of partial heating).

APPENDIX A TOOLS

A.1 DEVELOPMENT TOOLS

The following tools are provided for developing a system that uses the μPD78P368A:

Language processor

<table>
<tr><td>78K/III series relocatable assembler (RA78K3)</td><td colspan="4">This relocatable program can be used for all 78K/III series emulators. With its macro functions, it allows the user to improve program development efficiency. A structured-programming assembler is also provided, which enables explicit description of program control structures. This assembler could improve productivity in program production and maintenance.

<table>
<tr><th rowspan="2">Host machine</th><th colspan="2"></th><th rowspan="2">Part number</th></tr>
<tr><th>OS</th><th>Distribution media</th></tr>
<tr><td>PC-9800 series</td><td>MS-DOS™</td><td>3.5-inch 2HD</td><td>μS5A13RA78K3</td></tr>
<tr><td></td><td></td><td>5.25-inch 2HD</td><td>μS5A10RA78K3</td></tr>
<tr><td>IBM PC/AT™ or compatibles</td><td>PC DOS™</td><td>3.5-inch 2HC</td><td>μS7B13RA78K3</td></tr>
<tr><td></td><td></td><td>5.25-inch 2HC</td><td>μS7B10RA78K3</td></tr>
<tr><td>HP9000 series 700™</td><td>HP-UX™</td><td>DAT</td><td>μS3P16RA78K3</td></tr>
<tr><td>SPARCstation™</td><td>SunOS™</td><td>Cartridge tape (QIC-24)</td><td>μS3K15RA78K3</td></tr>
<tr><td>NEWS™</td><td>NEWS-OS™</td><td></td><td>μS3R15RA78K3</td></tr>
</table></td></tr>
<tr><td>78K/III series C compiler (CC78K3)</td><td colspan="4">This C compiler can be used for all 78K/III series emulators. The compiler converts programs written in C language into object codes executable on the microcomputer. When the compiler is used, the 78K/III series relocatable assembler package (RA78K3) is needed.

<table>
<tr><th rowspan="2">Host machine</th><th colspan="2"></th><th rowspan="2">Part number</th></tr>
<tr><th>OS</th><th>Distribution media</th></tr>
<tr><td>PC-9800 series</td><td>MS-DOS</td><td>3.5-inch 2HD</td><td>μS5A13CC78K3</td></tr>
<tr><td></td><td></td><td>5.25-inch 2HD</td><td>μS5A10CC78K3</td></tr>
<tr><td>IBM PC/AT or compatibles</td><td>PC DOS</td><td>3.5-inch 2HC</td><td>μS7B13CC78K3</td></tr>
<tr><td></td><td></td><td>5.25-inch 2HC</td><td>μS7B10CC78K3</td></tr>
<tr><td>HP9000 series 700</td><td>HP-UX</td><td>DAT</td><td>μS3P16CC78K3</td></tr>
<tr><td>SPARCstation</td><td>SunOS</td><td>Cartridge tape (QIC-24)</td><td>μS3K15CC78K3</td></tr>
<tr><td>NEWS</td><td>NEWS-OS</td><td></td><td>μS3R15CC78K3</td></tr>
</table></td></tr>
</table>

Remark It is guaranteed that the relocatable assembler and C compiler run only under the OSs on the corresponding host machines described above.

PROM programming tools

Hardware	PG-1500	The PG-1500 PROM programmer is used together with an accessory board and optional program adapter. It allows the user to program a single chip microcomputer containing PROM independently or from a host machine. The PG-1500 can be used to program typical 256K-bit to 4M-bit PROMs.
	PA-78P368GF PA-78P368KL	Programmer adapter for writing programs to the μPD78P368A. Used with a PROM programmer such as the PG-1500. PA-78P368GF : For μPD78P368AGF PA-78P368KL : For μPD78P368AKL
Software	PG-1500 controller	This program enables the host machine to control the PG-1500 through the serial and parallel interfaces.

Host machine	OS	Distribution media	Part number
PC-9800 series	MS-DOS	3.5-inch 2HD	μS5A13PG1500
		5.25-inch 2HD	μS5A10PG1500
IBM PC/AT or compatibles	PC DOS	3.5-inch 2HC	μS7B13PG1500
		5.25-inch 2HC	μS7B10PG1500

Remark It is guaranteed that the PG-1500 controller runs only under the OSs on the corresponding host machines described above.

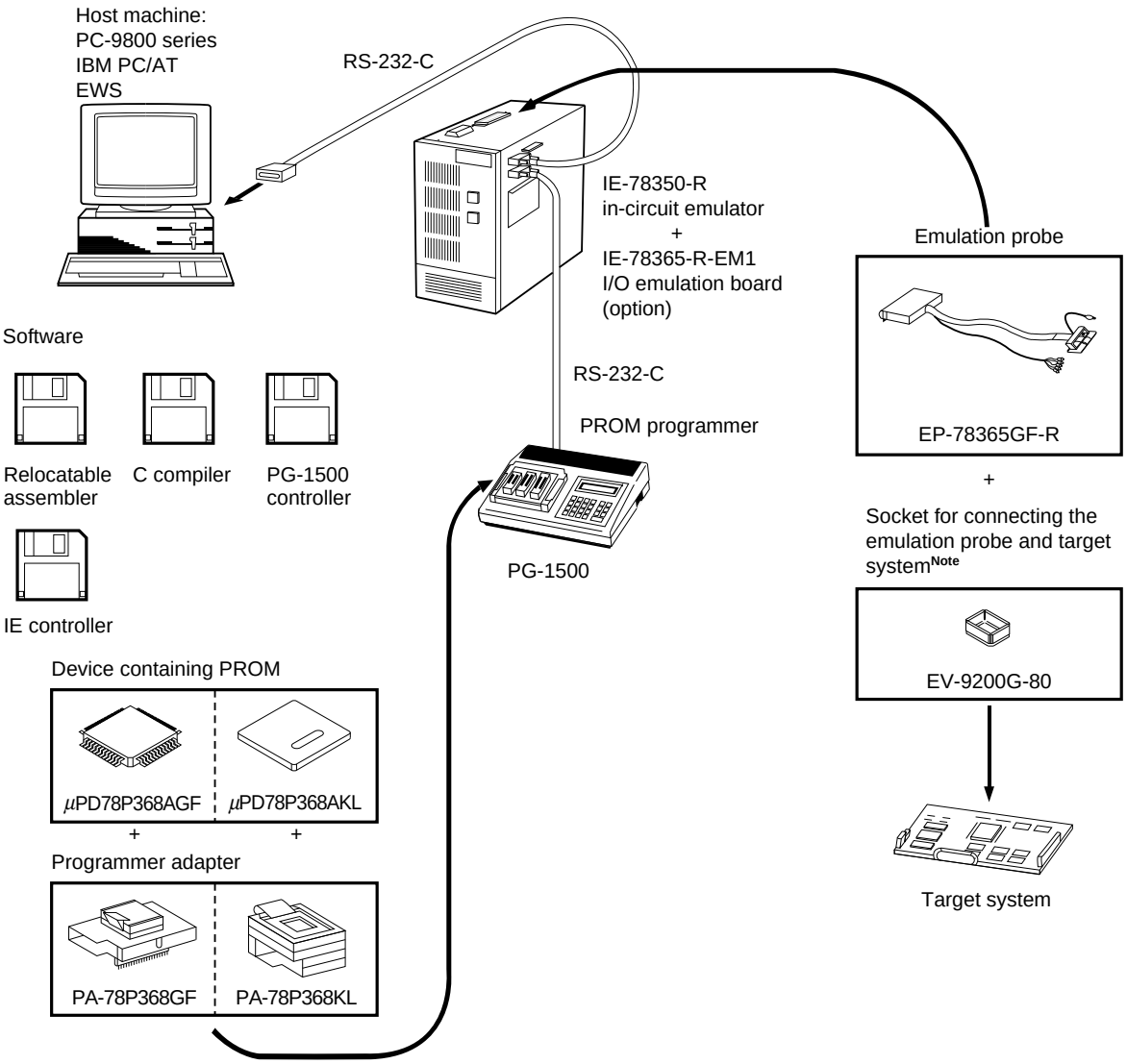
Debugging tools (when the IE controller is used)

Hardware	IE-78350-R	In-circuit emulator for developing and debugging an application system. For debugging, connect the emulator to the host machine.
	IE-78365-R-EM1	I/O emulation board for emulating peripheral hardware such as the I/O ports of the target device.
	EP-78365GF-R EV-9200G-80	Emulation probe for connecting the IE-78350-R to the target system. One EV-9200G-80 conversion socket is provided for connection to the target system.
Software	IE-78350-R control program (IE controller)	This control program allows the user to control the IE-78350-R from the host machine. Its automatic command execution function ensures more efficient debugging.

Host machine	OS	Distribution media	Part number	
PC-9800 series	MS-DOS	3.5-inch 2HD	μS5A13IE78365A	★
		5.25-inch 2HD	μS5A10IE78365A	★
IBM PC/AT or compatibles	PC DOS	3.5-inch 2HC	μS7B13IE78365A	★
		5.25-inch 2HC	μS7B10IE78365A	★

Remark It is guaranteed that the IE controller runs only under the OSs on the corresponding host machines described above.

Configuration of development tools (when the IE controller is used)



Note The socket is supplied with the emulation probe.

Remarks 1. The PG-1500 can be directly connected to the host machine via the RS-232-C interface.

2. In this figure, the distribution media of software is represented by the 3.5-inch floppy disk.

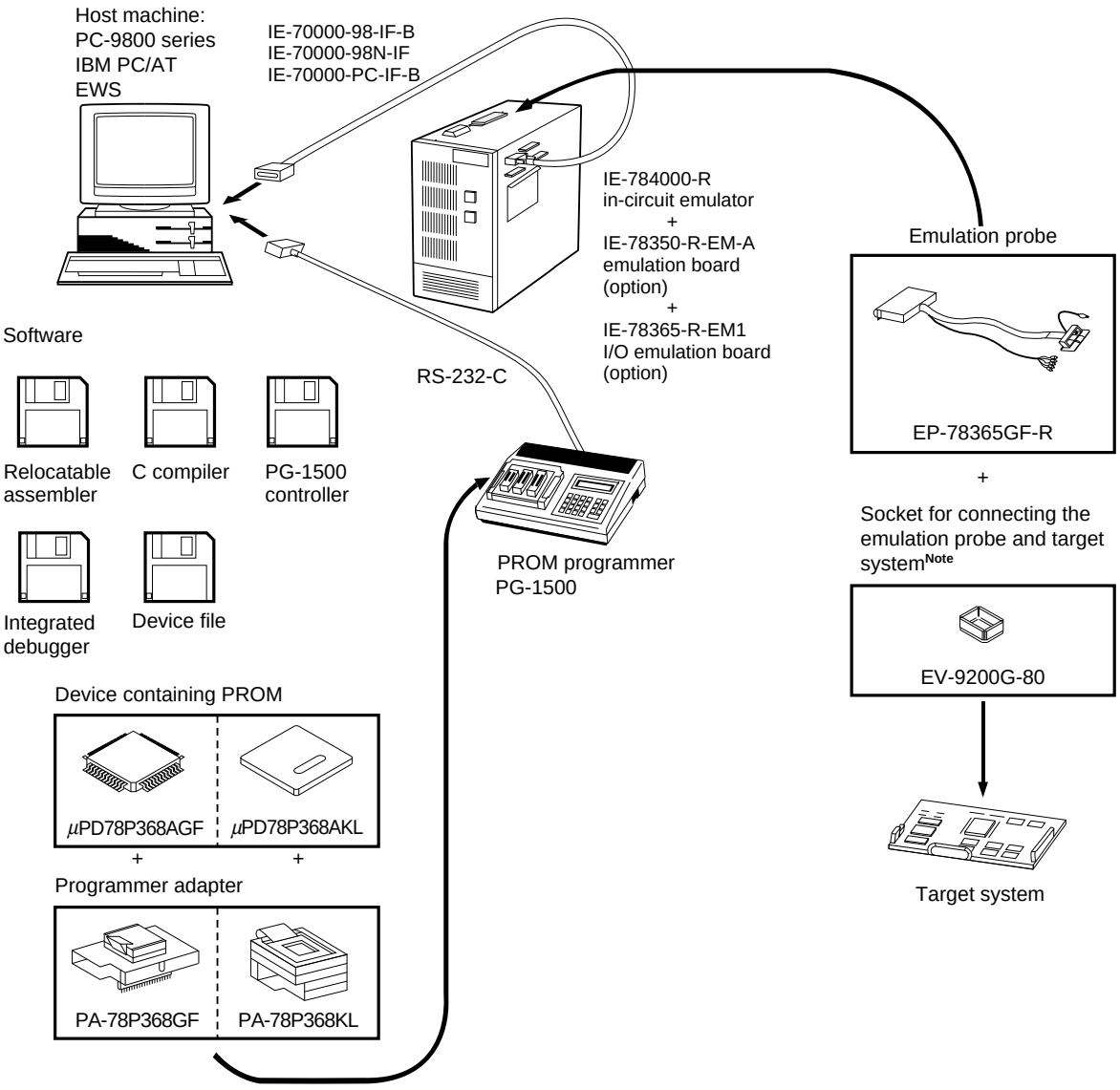
Debugging tools (when the integrated debugger is used)

<table>
<tr><td rowspan="9">Hardware</td><td>IE-784000-R</td><td colspan="4">In-circuit emulator for developing and debugging an application system. For debugging, connect the emulator to the host machine.</td></tr>
<tr><td>IE-78350-R-EM-ANote</td><td colspan="4">Emulation board for emulating peripheral hardware such as the I/O ports of the target device.</td></tr>
<tr><td>IE-78365-R-EM1</td><td colspan="4">I/O emulation board for emulating peripheral hardware such as the I/O ports of the target device.</td></tr>
<tr><td>EP-78365GF-R
EV-9200G-80</td><td colspan="4">Emulation probe for connecting the IE-784000-R to the target system. One EV-9200G-80 conversion socket is provided for connection to the target system.</td></tr>
<tr><td>IE-70000-98-IF-B</td><td colspan="4">Interface adapter when the PC-9800 series computer (other than a notebook) is used as the host machine.</td></tr>
<tr><td>IE-70000-98N-IF</td><td colspan="4">Interface adapter and cable when a PC-9800 series notebook is used as the host machine.</td></tr>
<tr><td>IE-70000-PC-IF-B</td><td colspan="4">Interface adapter when the IBM PC/AT is used as the host machine.</td></tr>
<tr><td>IE-78000-R-SV3</td><td colspan="4">Interface adapter and cable when the EWS is used as the host machine.</td></tr>
<tr><td rowspan="10">Software</td><td rowspan="6">Integrated debugger (ID78K3)</td><td colspan="4">Program for controlling the in-circuit emulator for the 78K/III series. The integrated debugger (ID78K3) is used together with the device file (DF78365).
Debugging can be performed for the source program written in C, structured assembly language, or assembly language. The ID78K3 can display various information simultaneously on the host machine screen divided into multiple areas. This ensures efficient debugging.</td></tr>
<tr><td rowspan="2">Host machine</td><td rowspan="2">OS</td><td rowspan="2">Distribution media</td><td rowspan="2">Part number</td></tr>
<tr></tr>
<tr><td>PC-9800 series</td><td>MS-DOS + Windows™</td><td>3.5-inch 2HD</td><td>μSAA13ID78K3</td></tr>
<tr><td></td><td></td><td>5.25-inch 2HD</td><td>μSAA10ID78K3</td></tr>
<tr><td>IBM PC/AT or compatibles (Japanese Windows)</td><td rowspan="2">PC DOS + Windows</td><td>3.5-inch 2HC</td><td>μSAB13ID78K3</td></tr>
<tr><td></td><td>5.25-inch 2HC</td><td>μSAB10ID78K3</td></tr>
<tr><td>IBM PC/AT or compatibles (Windows)</td><td>3.5-inch 2HC</td><td>μSBB13ID78K3</td></tr>
<tr><td></td><td></td><td>5.25-inch 2HC</td><td>μSBB10ID78K3</td></tr>
<tr><td rowspan="6">Device file (DF78365)</td><td colspan="4">File which contains the device-specific information. The device file (DF78365) is used together with the assembler (RA78K3), C compiler (CC78K3), or integrated debugger (ID78K3).</td></tr>
<tr><td rowspan="2">Host machine</td><td rowspan="2">OS</td><td rowspan="2">Distribution media</td><td rowspan="2">Part number</td></tr>
<tr></tr>
<tr><td>PC-9800 series</td><td>MS-DOS</td><td>3.5-inch 2HD</td><td>μS5A13DF78365</td></tr>
<tr><td></td><td></td><td>5.25-inch 2HD</td><td>μS5A10DF78365</td></tr>
<tr><td>IBM PC/AT or compatibles</td><td>PC DOS</td><td>3.5-inch 2HC</td><td>μS7B13DF78365</td></tr>
<tr><td></td><td></td><td>5.25-inch 2HC</td><td>μS7B10DF78365</td></tr>
</table>

Note Under development

Remark It is guaranteed that the integrated debugger and device file run only under the OSs on the corresponding host machines described above.

Configuration of development tools (when the integrated debugger is used)



Note The socket is supplied with the emulation probe.

Remarks 1. In this figure, the host machine is represented by the desktop personal computer.

2. In this figure, the distribution media of software is represented by the 3.5-inch floppy disk.

A.2 EMBEDDED SOFTWARE

To improve the efficiency of program development and simplify the maintenance of systems incorporating this microcontroller, the following embedded software is provided.

Real-time OS

<table>
<tr><td rowspan="5">Real-time OS
(RX78K/III)Note</td><td colspan="3">This operating system was designed to provide a multitasking environment for control applications that require real-time processing. System performance is improved by using the idling CPU for other processing.
RX78K/III provides system calls that conform to μITRON specifications.
The RX78K/III package provides the RX78K/III nucleus and a tool (Configurator) that is used for creating multiple information tables.</td></tr>
<tr><td rowspan="2">Host machine</td><td colspan="2" rowspan="2">Part number</td></tr>
<tr><td>OS</td></tr>
<tr><td>PC-9800 series</td><td>MS-DOS</td><td>3.5-inch 2HD</td><td>Undecided</td></tr>
<tr><td></td><td></td><td>5.25-inch 2HD</td><td>Undecided</td></tr>
<tr><td>IBM PC/AT or compatibles</td><td>PC DOS</td><td>3.5-inch 2HC</td><td>Undecided</td></tr>
<tr><td></td><td></td><td>5.25-inch 2HC</td><td>Undecided</td></tr>
</table>

Note Under development

Caution Before purchasing this software, complete the purchase application sheet and sign the software license agreement.

Remark To use the RX78K/III real-time operating system, the optional RA78K3 assembler package is required.

Fuzzy inference development support system

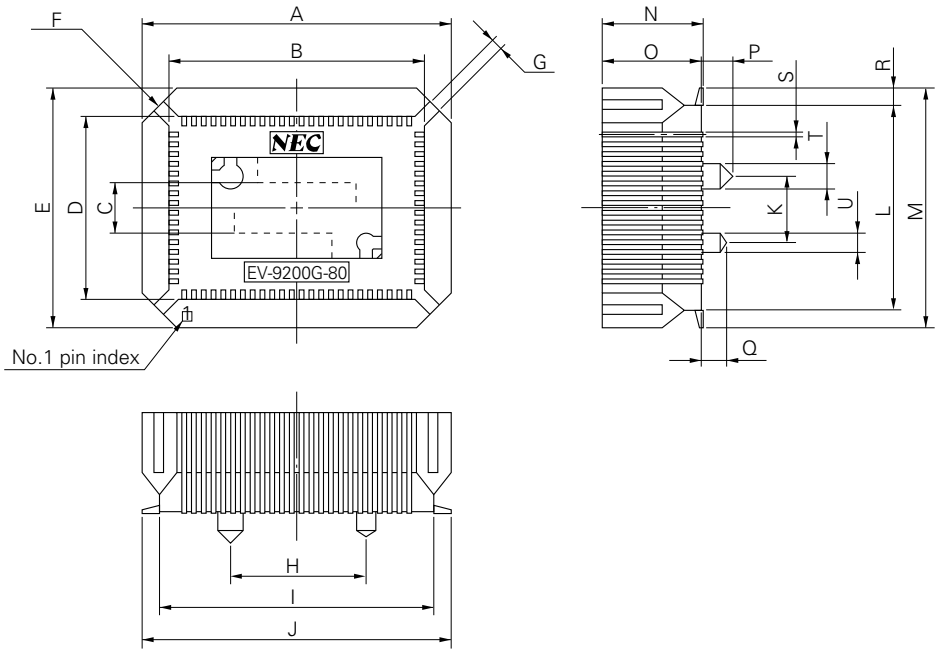
Tool for creating fuzzy knowledge data (FE9000, FE9200)	This program supports the input/editing and simulation of fuzzy knowledge data (fuzzy rules and membership functions).			
	Host machine	OS	Distribution media	Part number
	PC-9800 series	MS-DOS	3.5-inch 2HD	μS5A13FE9000
			5.25-inch 2HD	μS5A10FE9000
	IBM PC/AT or compatibles	PC DOS + Windows	3.5-inch 2HC	μS7B13FE9200
			5.25-inch 2HC	μS7B10FE9200
Translator (FT78K3)Note	This program converts fuzzy knowledge data, obtained using the tool for creating fuzzy knowledge data, into an assembler source program for RA78K3.			
	Host machine	OS	Distribution media	Part number
	PC-9800 series	MS-DOS	3.5-inch 2HD	μS5A13FT78K3
			5.25-inch 2HD	μS5A10FT78K3
	IBM PC/AT or compatibles	PC DOS	3.5-inch 2HC	μS7B13FT78K3
			5.25-inch 2HC	μS7B10FT78K3
Fuzzy inference module (FI78K/III)Note	This program performs fuzzy inference by linking the fuzzy knowledge data converted by Translator.			
	Host machine	OS	Distribution media	Part number
	PC-9800 series	MS-DOS	3.5-inch 2HD	μS5A13FI78K3
			5.25-inch 2HD	μS5A10FI78K3
	IBM PC/AT or compatibles	PC DOS	3.5-inch 2HC	μS7B13FI78K3
			5.25-inch 2HC	μS7B10FI78K3
Fuzzy inference debugger (FD78K/III)	This software supports the evaluation and adjustment of fuzzy knowledge data at the hardware level, by using an in-circuit emulator.			
	Host machine	OS	Distribution media	Part number
	PC-9800 series	MS-DOS	3.5-inch 2HD	μS5A13FD78K3
			5.25-inch 2HD	μS5A10FD78K3
	IBM PC/AT or compatibles	PC DOS	3.5-inch 2HC	μS7B13FD78K3
			5.25-inch 2HC	μS7B10FD78K3

Note Under development

APPENDIX B DIMENSIONS OF THE CONVERSION SOCKET AND RECOMMENDED PATTERN ON BOARDS

Fig. B-1 Dimensions of the Conversion Socket (EV-9200G-80)(Reference)

Based on EV-9200G-80
(1) Package drawing (in mm)

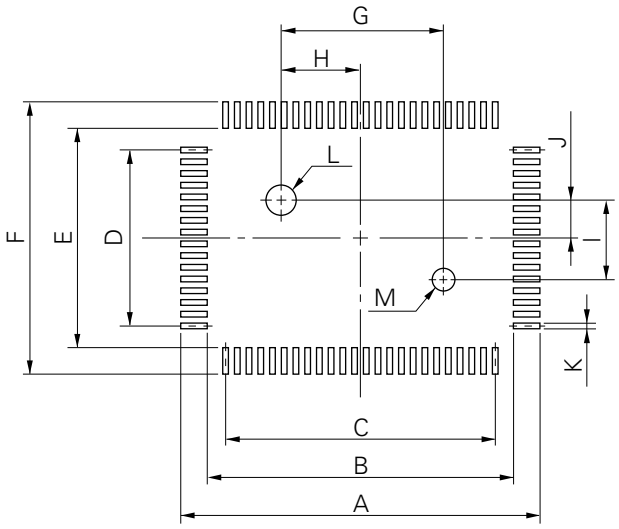


EV-9200G-80-G0

ITEM	MILLIMETERS	INCHES
A	25.0	0.984
B	20.30	0.799
C	4.0	0.157
D	14.45	0.569
E	19.0	0.748
F	4-C 2.8	4-C 0.11
G	0.8	0.031
H	11.0	0.433
I	22.0	0.866
J	24.7	0.972
K	5.0	0.197
L	16.2	0.638
M	18.9	0.744
O	8.0	0.315
N	7.8	0.307
P	2.5	0.098
Q	2.0	0.079
R	1.35	0.053
S	0.35±0.1	$0.014^{+0.004}_{-0.005}$
T	φ2.3	φ0.091
U	φ1.5	φ0.059

Fig. B-2 Recommended Pattern on Boards for the Conversion Socket (EV-9200G-80)(Reference)

Based on EV-9200G-80
(2) Pad drawing (in mm)



EV-9200G-80-P0

ITEM	MILLIMETERS	INCHES
A	25.7	1.012
B	21.0	0.827
C	$0.8\pm0.02\times23=18.4\pm0.05$	$0.031^{+0.002}_{-0.001}\times0.906=0.724^{+0.003}_{-0.002}$
D	$0.8\pm0.02\times15=12.0\pm0.05$	$0.031^{+0.002}_{-0.001}\times0.591=0.472^{+0.003}_{-0.002}$
E	15.2	0.598
F	19.9	0.783
G	11.00 ± 0.08	$0.433^{+0.004}_{-0.003}$
H	5.50 ± 0.03	$0.217^{+0.001}_{-0.002}$
I	5.00 ± 0.08	$0.197^{+0.003}_{-0.004}$
J	2.50 ± 0.03	$0.098^{+0.002}_{-0.001}$
K	0.5 ± 0.02	$0.02^{+0.001}_{-0.002}$
L	$\phi2.36\pm0.03$	$\phi0.093^{+0.001}_{-0.002}$
M	$\phi1.57\pm0.03$	$\phi0.062^{+0.001}_{-0.002}$

Caution Dimensions of mount pad for EV-9200 and that for target device (QFP) may be different in some parts. For the recommended mount pad dimensions for QFP, refer to "SEMICONDUCTOR DEVICE MOUNTING TECHNOLOGY MANUAL" (IEI-1207).

Cautions on CMOS Devices

☒ Countermeasures against static electricity for all MOSs

Caution When handling MOS devices, take care so that they are not electrostatically charged.

Strong static electricity may cause dielectric breakdown in gates. When transporting or storing MOS devices, use conductive trays, magazine cases, shock absorbers, or metal cases that NEC uses for packaging and shipping. Be sure to ground MOS devices during assembling. Do not allow MOS devices to stand on plastic plates or do not touch pins.

Also handle boards on which MOS devices are mounted in the same way.

☒ CMOS-specific handling of unused input pins

Caution Hold CMOS devices at a fixed input level.

Unlike bipolar or NMOS devices, if a CMOS device is operated with no input, an intermediate-level input may be caused by noise. This allows current to flow in the CMOS device, resulting in a malfunction. Use a pull-up or pull-down resistor to hold a fixed input level. Since unused pins may function as output pins at unexpected times, each unused pin should be separately connected to the V_{DD} or GND pin through a resistor.

If handling of unused pins is documented, follow the instructions in the document.

☒ Statuses of all MOS devices at initialization

Caution The initial status of a MOS device is unpredictable when power is turned on.

Since characteristics of a MOS device are determined by the amount of ions implanted in molecules, the initial status cannot be determined in the manufacture process. NEC has no responsibility for the output statuses of pins, input and output settings, and the contents of registers at power on. However, NEC assures operation after reset and items for mode setting if they are defined.

When you turn on a device having a reset function, be sure to reset the device first.

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